Speedcore DFT and Test User Guide (UG067)

Speedcore eFPGA



Copyrights, Trademarks and Disclaimers

Copyright © 2021 Achronix Semiconductor Corporation. All rights reserved. Achronix, Speedcore, Speedster, and ACE are trademarks of Achronix Semiconductor Corporation in the U.S. and/or other countries All other trademarks are the property of their respective owners. All specifications subject to change without notice.

NOTICE of DISCLAIMER: The information given in this document is believed to be accurate and reliable. However, Achronix Semiconductor Corporation does not give any representations or warranties as to the completeness or accuracy of such information and shall have no liability for the use of the information contained herein. Achronix Semiconductor Corporation reserves the right to make changes to this document and the information contained herein at any time and without notice. All Achronix trademarks, registered trademarks, disclaimers and patents are listed at http://www.achronix.com/legal.

Achronix Semiconductor Corporation

2903 Bunker Hill Lane Santa Clara, CA 95054 USA

Website: www.achronix.com E-mail: info@achronix.com

Table of Contents

Chapter - 1: Overview	6
Chapter - 2: Test Coverage and Cost	7
Chapter - 3: DFT Features	9
Scan-Accessible ASIC Logic	9
Boundary Loopbacks	9
Shallow Reverse Loopback	
Deep Reverse Loopback	
Deep Fabric Combinational Loopback	
Error Insertion into ECC Logic	
Bypass CMEM Clear Mode	
Gated I/O	
SRAM Yield Analysis	14
Chapter - 4: DFT Methodologies	15
Custom Tests	15
ASIC Scan Tests	
Memory Tests	
BRAM EMA	
Loopbacks for Interface Tests	17
Fault Diagnostics	17
Chapter - 5: Deliverables, Requirements and Testing	18
Methodology and Coverage Deliverables	18
ATE Test System	18
Customer Implementation Requirements	18
Scan Chain Bus for Speedcore eFPGAs	
Speedcore Pins Used in DFT Modes	
Usage Scenarios	
Potential SoC-level Pin-Count Reduction	
Numing Oser Froundment resis	2/

Speedcore DFT and Test User Guide (UG067)			
Revision History		3(

Protected Document

The full contents of this document are confidential and require a signed non-disclosure agreement (NDA) between Achronix and your company. Talk with your Achronix sales representative about obtaining an NDA.

Gaining access to Achronix confidential design documents requires the following steps:

- 1. Ensure that your company/organization has an active NDA with Achronix.
- 2. Log into your Achronix support portal account. If you do not yet have a support portal account, please refer to "How Do I Register for an Achronix Support Account" to register and set up your account.
- 3. When logged in, click the link "Submit a request" located next to your user name.
- 4. Select Document Request under Submit a request.

Submit a request

Please choose your issue below

_

General Support Issue

ACE License Request

Document Request

Synplify Pro License Refresh Request

- 5. When the ticket form is selected, a number of ticket fields are revealed. Enter a description of the document(s) you are wanting to access, and click **Submit** when complete.
- 6. A support engineer will review your request and, if approved, will grant you access to the documents/files.

Note

The fields, Subject and Description are not meaningful for the process, but are nevertheless required to submit the ticket.