Getting Started User Guide (UG105)

All Achronix Devices

Achronix
Data Acceleration

Copyrights, Trademarks and Disclaimers

Notice of Disclaimer

The information given in this document is believed to be accurate and reliable. However, Achronix Semiconductor Corporation does not give any representations or warranties as to the completeness or accuracy of such information and shall have no liability for the use of the information contained herein. Achronix Semiconductor Corporation reserves the right to make changes to this document and the information contained herein at any time and without notice. All Achronix trademarks, registered trademarks, disclaimers and patents are listed at http://www.achronix.com/legal.

Achronix Semiconductor Corporation

2903 Bunker Hill Lane
Santa Clara, CA 95054
USA

Website: www.achronix.com
E-mail : info@achronix.com

Table of Contents

Chapter 1 : Overview

This guide serves as a concise introduction to the Achronix tools flow. After an overview of the tools and IP flow, the quickstart design included with all ACE installations is used to illustrate the tool flow.

The Achronix design flow is composed of the following software tools:

- ACE – used for IP configuration, place-and-route of the design, timing analysis, and bitstream generation. ACE includes flow steps to run synthesis and simulation, which run third-party tools under the hood
- Synplify Pro – used for design synthesis
- Simulation tools – Achronix libraries support Synopsys VCS, Aldec Riviera, Mentor QuestaSim, and Cadence Xcelium

Synplify Pro operates in GUI and batch modes and ACE operates in GUI, command-line, and batch modes.

> **Note**
>
> This user guide assumes that one of the supported simulation tools, Synplify Pro, and ACE are already installed. For help installing the tools or if issues are being encountered, such as problems with launching the tools or the desired device is missing, see the ***ACE Installation and Licensing Guide*** (UG002)[1].

The following documents provide additional information on topics covered in this guide:

- ***Synthesis User Guide*** (UG018)[2]
- ***ACE User Guide*** (UG070)[3]

The following document provides useful information on topics not covered in this guide:

- ***Simulation User Guide*** (UG072)[4]

1 https://www.achronix.com/documentation/ace-installation-and-licensing-guide-ug002
2 https://www.achronix.com/documentation/synthesis-user-guide-ug018
3 https://www.achronix.com/documentation/ace-user-guide-ug070
4 https://www.achronix.com/documentation/simulation-user-guide-ug072

Chapter 2 : Achronix Tool Flow

Tool Flow Overview

The Achronix design flow is composed of the following software tools:

- ACE – used for IP configuration, place-and-route of the design, timing analysis, and bitstream generation. ACE includes flow steps to run synthesis and simulation, which run third-party tools under the hood.
- Synplify Pro – used for design synthesis. Synplify Pro can be run stand-alone outside of ACE, or from within ACE as part of the Run Synthesis flow step.
- Simulation tools - Achronix libraries support Synopsys VCS, Aldec Riviera, Mentor QuestaSim, and Cadence Xcelium. Simulators can be run stand-alone outside of ACE, or from within ACE as part of the simulation flow steps.

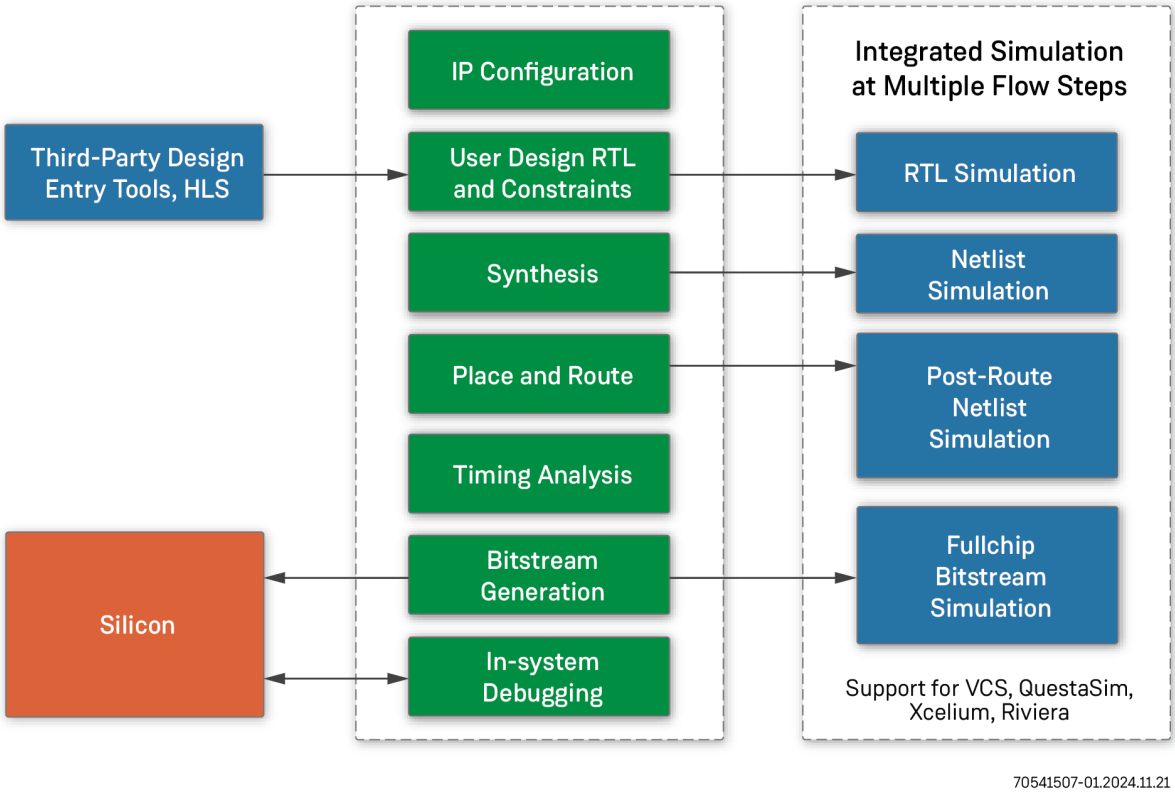


Figure 1 • Achronix Design Flow

IP Configuration Flows

Achronix offers two types of IP configuration flows:

- Core IP (also known as soft IP) – Parameterized synthesizable RTL macros which can be configured and instantiated in the end user design RTL and mapped into the FPGA fabric.
- I/O Ring IP (also known as hard IP) – The I/O ring holds the various interface subsystems (hard IP controllers, PLLs, I/O, and more) that surround the FPGA core.

Core IP Design Flow

Achronix provides a device-specific library of core IP for each Speedster or Speedcore device. Each core IP can be configured by manually instantiating the core IP RTL macro and setting its parameters, or by using the built-in IP Configuration GUI tools in ACE. When using the ACE GUI tools:

1. Create or load and ACE Project
2. Ensure the correct target device is selected in the ACE project options
3. Navigate to the IP Configuration Perspective in the GUI
4. In the IP Libraries View, select the type of core IP to configure and create a new IP Configuration (`*.acxip` file)
5. Configure the IP in the IP Configuration Editor. The editor will perform design rule checks on the configuration.
6. Once you have an IP Configuration that meets your needs and passes all design rule checks, generate IP design files for the desired IP configuration by clicking **Generate**.
7. In the Generate IP Design Files dialog, select the output files you wish to generate. At a minimum, the Verilog or SystemVerilog file must be generated.
8. The generated RTL and constraints file outputs can then be used in the end user RTL design, just like any other RTL module and constraints. A generated IP module may be instantiated one or more times in the design. These output files are inputs to Synthesis and Place and Route flow steps.

See the ***Speedster7t Soft IP User Guide*** (UG103)[5] and ***Speedcore Soft IP User Guide*** (UG113)[6] for details.

I/O Ring IP Design Flow

For Speedster instance, Achronix provides a device simulation model (DSM) for the entire I/O ring and a suite of I/O ring IP configuration tools, which are referred to as the I/O Designer Toolkit. The end user design RTL is mapped to the FPGA fabric, and does not instantiate any I/O ring blocks. Instead, the end user design RTL interfaces to the IO ring (modeled with the DSM in simulation), and the I/O ring is simply "configured" using the I/O Designer Toolkit in ACE. The I/O Ring configuration involves the following:

1. Create or load and ACE Project
2. Ensure the correct target device is selected in the ACE project options
3. Navigate to the IP Configuration Perspective in the GUI
4. In the IP Libraries View, select the type of I/O ring IP to configure and create a new IP Configuration (`*.acxip` file), or double-click the desired IP for configuration in the I/O Layout Diagram View

5 https://www.achronix.com/documentation/speedster7t-soft-ip-user-guide-ug103
6 https://www.achronix.com/documentation/speedcore-soft-ip-user-guide-ug113

5. Configure the IP in the IP Configuration Editor. The editor will perform design rule checks on the configuration.

> **Note**
>
> The I/O ring IP design rule checks not only check the rules of the specific IP being configuring, but also perform system/chip-level cross checks against other IP and shared resources such as the clock and reset networks. Sometimes it is necessary to configure multiple I/O ring IP to satisfy all the design rule checks. For example, to properly configure a GDDR6, the following must also be configured: 2D NoC, a PLL to drive the reference clocks, and a CLKIO to drive the PLL. The I/O Designer toolkit provides helpful messages to guide users through the process.

6. Once the entire I/O ring configuration passes all design rule checks, generate the I/O ring design files for the project by clicking **Generate I/O Ring Design Files**. Check the checkbox to automatically add the required output files to the ACE project. The I/O ring design file generation outputs several files, including:
   a. The bitstream for the I/O ring
   b. Simulation configuration files
   c. Top-level user design port list
   d. ACE boundary timing and pin placement constraints for place and route
   e. I/O ping power and utilization XML

   The generated output files are inputs to simulation and place and route.

See the user guides for each I/O ring interface subsystem for details on configuration, for example, the chapter, "GDDR6 IP Software Support in ACE" in the ***Speedster7t GDDR6 User Guide*** (UG091)[7].

7 https://www.achronix.com/documentation/speedster7t-gddr6-user-guide-ug091

Chapter 3 : Launching Synplify Pro

Synplify Pro can be run in either the GUI or batch mode. Refer to the ***ACE Installation and Licensing Guide*** (UG002)[8] for details on installing Synplify Pro and ***Synthesis User Guide*** (UG018)[9] for more details on synthesis.

> **Note**
>
> To list the several options available when launching Synplify Pro, use the `-h` argument with the `synplify_pro` command.

Using the Built-in ACE Flow Step

As of ACE 10.0, ACE now provides a Run Synthesis flow step, which can be used to configure and call Synplify Pro directly to help streamline the end user tools flow experience. Synplify Pro must be installed in a directory accessible from the computer on which ACE is running.

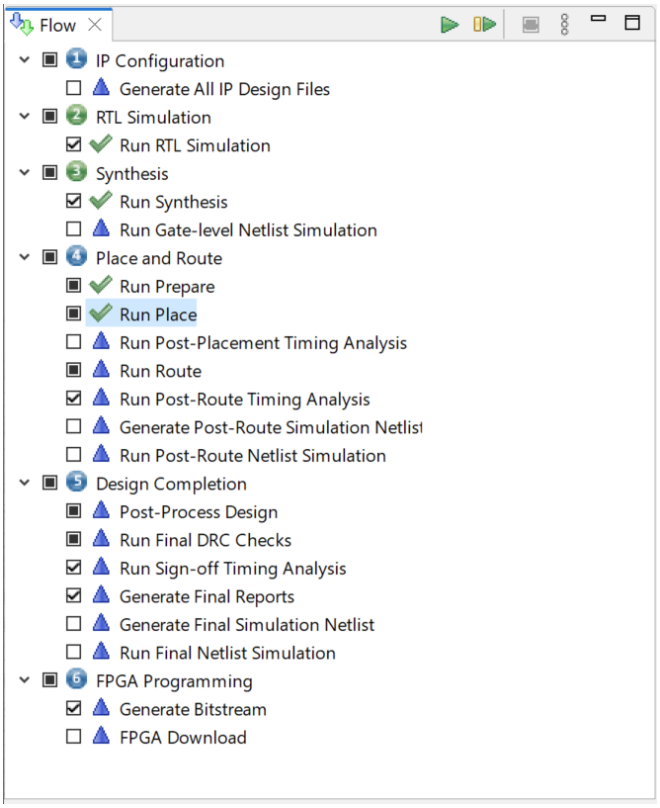
As of ACE 10.2, it is no longer necessary to set the $ACX_SYNPLIFY_TOOL_PATH environment variable. ACE now searches for the Synplify Pro installation according to the following order of precedence:

1. If ACX_SYNPLIFY_TOOL_PATH is set, use it
2. Otherwise, check if $SYNPLIFY_HOME is set, and search for it there
3. Otherwise, check to see if Synplify Pro is available inside the ACE install at <ace_install>/Synplify/bin/synplify_pro(.exe on Windows). This option is the recommended default.
4. Otherwise, check to see if Synplify Pro is available on the $PATH environment variable
5. Otherwise, error out

To run synthesis in ACE, simply:

1. Add the source user design RTL and synthesis constraints to the ACE project
2. Configure the synthesis implementation options for the ACE project
3. In the ACE Flow View, simply check the box next to the Run Synthesis flow step to enable it
4. Run the flow in ACE

8 https://www.achronix.com/documentation/ace-installation-and-licensing-guide-ug002
9 https://www.achronix.com/documentation/synthesis-user-guide-ug018



GUI Mode

If a Synplify Pro shortcut or alias was not created, see the following table for the path to the program file.

Table 1 • Synplify Pro File Paths

Executable File	Typical Windows Path	Typical Linux Path
`synplify_pro`	`<ace_install_dir>\Synplify\bin`	`<ace_install_dir>/Synplify/bin`

When executed, the following window is displayed:

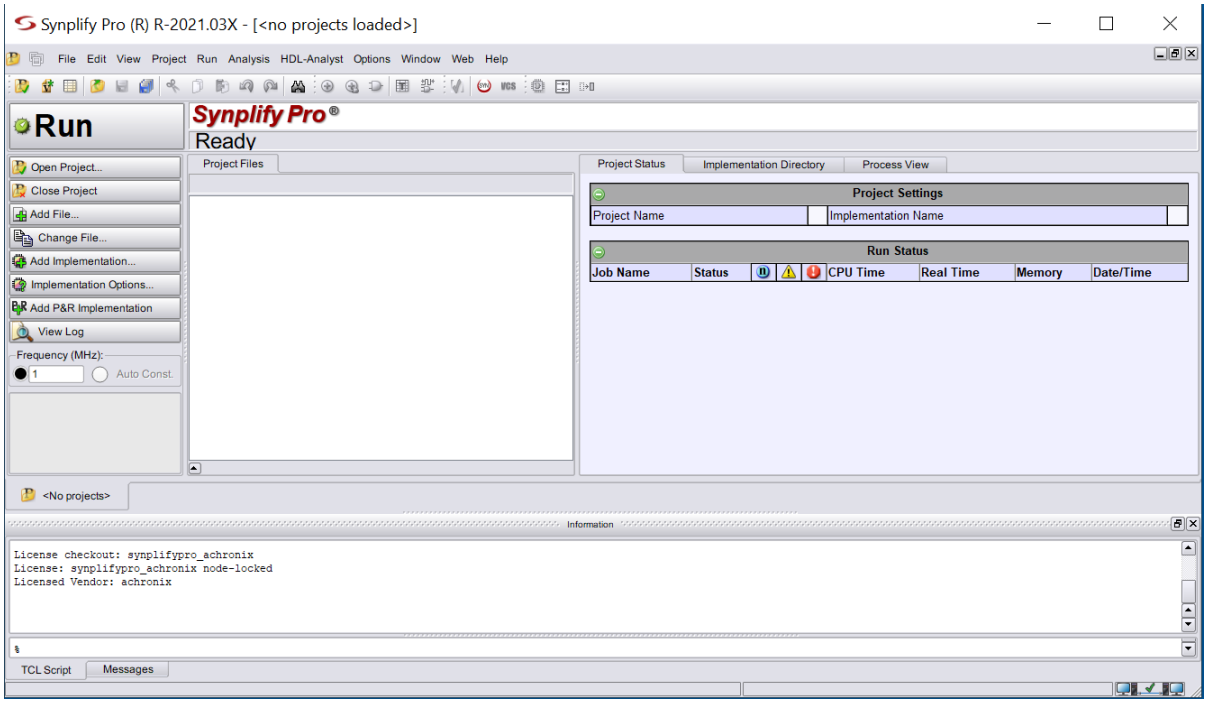


Figure 2 • Synplify Pro Opening Display

Batch Mode

To run Synplify Pro in batch mode, use the `-batch` argument with the `synplify_pro` command. Reference designs support batch mode and have specific scripts for batch runs.

> **Note**
>
> A floating license is required in order to use batch mode with Synplify Pro.

Chapter 4 : Launching ACE

ACE Execution Modes

ACE can be run with full functionality in three different modes:

- GUI Mode
- Command-line Mode
- Batch Mode

For details beyond that covered in this guide, refer to the ***ACE User Guide*** **(UG070)**[10].

GUI Mode

If an ACE shortcut or alias does not exist, see the following table for the path to the executable program file.

Table 2 • ACE Program File Path

Executable File	Typical Windows Path	Typical Linux Path
`ace`	`C:\Program Files\Achronix CAD Environment\Achronix`	`<install_path>/Achronix-linux`

To run in GUI mode, invoke the `ace` executable either with no options or with the `-gui` option. GUI mode launches the interactive window from which all commands are issued.

Starting ACE in GUI Mode, Implicit

```
% ./ace
```

or

Starting ACE in GUI Mode, Explicit

```
% ./ace -gui
```

10 https://www.achronix.com/documentation/ace-user-guide-ug070

Command-line Mode

To run in command-line mode, invoke the `ace` executable with the `-b` option from a console. Command-line mode takes control of the console and allows interactive entry of Tcl commands at the command prompt.

Starting ACE in Command-line Mode

```
% ./ace -b
-- ACE -- Achronix CAD Environment -- Version 5.4 -- Build  84486- -- Date 2015-02-11 19:5
8
-- (c) Copyright 2006-2015 Achronix Semiconductor Corp.  All rights reserved.
-- all messages logged in file /home/username/.achronix/ace_2015_02_13_11_00_11.log,
created at 11:00:11 on 02/13/2015
INFO: License ace-v1.0 on server acxlicense (9 of 10 licenses available). Running on
docs.achronix.local (x86_64).
ACE>
```

Batch Mode

To run in batch mode, invoke the `ace` executable with the `-b` option and the `-script_file` option. Reference designs support batch mode and have scripts to refer to as examples.

Starting ACE in Batch Mode

```
% ./ace -b -script_file <path_to_script_file>.tcl
```

Chapter 5 : The Quickstart Design

Introduction

The simple Quickstart design features a 2-bit binary up-counting LED display to indicate that the board and FPGA are operating properly upon powerup. The Quickstart design RTL along with the device-specific netlists and constraints are available under the `<ACE_install_dir>Achronix/examples/quickstart` directory.

While this tutorial is intended to help gain familiarity with the tools flow, some details are omitted to keep it concise. See the ***ACE User Guide*** **(UG070)**[11], ***Synthesis User Guide*** **(UG018)**[12], and **Simulation User Guide (UG072)**[13] for additional details and alternate flows.

Running the Quickstart Design Through the Tools

Start by copying all the files from `<ace_install_dir>/examples/quickstart/<device>` into a new empty directory (`<test_dir>`) in your file system. Use the `<device>` directory that matches the target device implementation option selected in step 2. Before launching ACE, make sure to install Synplify Pro and your Simulation tools, and configured the environment variables (such as `$ACX_SYNPLIFY_TOOL_PATH` and `$ACX_<sim_tool>_TOOL_PATH`) by following the instructions in the ***ACE Installation and Licensing Guide*** **(UG002)**[14].

Follow these simple steps to complete your first design in ACE:

1. Create the Project

In the Projects View, click the ( ) **Create Project** toolbar button. Follow these steps to create the project:

1. In the Create Project Dialog, enter (or browse to) the path to `<test_dir>` in the Project Directory field.
2. Enter `quickstart` in the **Project Name** field and click **OK**.

You should now see your new project show up in the Projects view. See Creating Projects or Working with Projects and Implementations for more details.

2. Add the Design Files and Set Implementation Options

In the Projects view, click the "quickstart" project to select it. Follow these steps to add the design source files for Simulation, Synthesis, and Place and Route:

1. Click the ( ) **Add Source Files** toolbar button and select **Add RTL Files**.
2. In the Add RTL Files dialog, browse to the `<test_dir>/src/rtl` directory and select all of the files by holding down the **CTRL** key and clicking each file name.

11 https://www.achronix.com/documentation/ace-user-guide-ug070
12 https://www.achronix.com/documentation/synthesis-user-guide-ug018
13 https://www.achronix.com/documentation/simulation-user-guide-ug072
14 https://www.achronix.com/documentation/ace-installation-and-licensing-guide-ug002

3. Click the **Open** button to add the RTL files to your project.
4. Click the ( ) **Add Source Files** toolbar button and select **Add Synthesis Constraint Files**.
5. In the Add Synthesis Constraint Files dialog, browse to the `<test_dir>/src/constraints` directory and click the `quickstart.sdc` file to select it.
6. Click the **Open** button to add the Synthesis Constraint files to your project.
7. Click the ( ) **Add Source Files** toolbar button and select **Add Place and Route Constraint Files**.
8. In the Add Place and Route Constraint Files dialog, browse to the `<test_dir>/src/constraints` directory and select all of the files by holding down the **CTRL** key and clicking each file name.
9. Click the **Open** button to add the place and route constraint files to your project.
10. Click the ( ) **Add Source Files** toolbar button and select **Add Simulation Testbench Files**.
11. In the Add Simulation Testbench Files dialog, browse to the `<test_dir>/src/tb` directory and select all of the files by holding down the **CTRL** key and clicking each file name.
12. Click the **Open** button to add the simulation testbench files to your project.

In the Options View, follow these steps to configure your project options:

1. Expand the **Project Options** section and select the **Target Device** that matches the set of design files that you copied earlier.
2. In the **Project Options** section, scroll down and enter the following semicolon-separated list for the **HDL Include Path**:
   - `<test_dir>/src/rtl;<test_dir>/src/tb`

   Note: The **HDL Include Path** applies to both **Synthesis** and **Simulation**.
3. Scroll down and expand the **Simulation** section of options.
4. Select the **Simulation Tool** you have installed from the drop-down list and enter `tb_quickstart` for the **Testbench Top Module**.

You now have a project that is ready to run through the flow! See Adding Source Files or Working with Projects and Implementations for more details.

3. Run the Flow

1. In the Flow view, expand the tree to view the detailed flow steps.
2. Under **RTL Simulation**, click the checkbox next to **Run RTL Simulation**.
3. Click the ( ) **Run Flow** toolbar button.

Textual output from the flow is shown in the Tcl Console view. When the flow is finished running, you can see the completed flow steps in the Flow view updated with a green check mark ( ) to indicate success, and all newly generated reports are displayed in the editor area. See the Flow concept or Running the Flow for more details.

4. Analyze the Results

1. On the main toolbar, click the ( ) **Floorplanner Perspective** toolbar button.

2. Within this perspective, use the Critical Paths View to analyze critical paths and highlight them in the Floorplanner View. Clicking the () **Zoom To Path** toolbar button in the Critical Paths view, zooms the Floorplanner View to the path currently selected in the Critical Paths view.
3. Use the Search View and Selection View to locate objects of interest.

Clicking the () **Zoom To Selection** toolbar button in the Selection view zooms the Floorplanner view to the objects in the current selection set. See the Viewing the Floorplanner and Analyzing Critical Paths tasks in the User Guide for more details.

Congratulations!!!

You have successfully completed a design in ACE!

Chapter 6 : FAQs

Why is my Device not Listed in Synplify Pro or ACE?

The most likely cause is likely because the device overlay was not correctly installed. See ***ACE Installation and Licensing Guide*** **(UG002)**[15].

Which Simulators are Supported?

VCS (Synopsys), QuestaSim (Mentor), Xcelium (Cadence), and Riviera (Aldec). Achronix does not distribute or provide these simulator tools.

I am in a Perspective, but I Would Like to Add a Window from a Different Perspective. How do I do This?

Most windows can be added by selecting **Window** → **Show View** from the menu. Select the desired window or select **Other** to see all windows that can be added.

I Loaded an ACE Project, but the Information on its Implementation is Missing. How do I Get that Information?

Loading/restoring an ACE project does not load the binary database of place-and-route data from session's implementation run. After loading/restoring the project, right-click the implementation and select **Restore Implementation** to load the place-and-route data which was saved to a binary `*.acxdb` file during the previous run through the Place and Route flow.

How can I Drive or Observe Signals When my Device is Running?

The Snapshot Debugger, found within ACE, can both drive and observe signals. See ***Snapshot User Guide*** **UG016**[16] for more details.

I am Stuck and my Question is not Shown Here. Whom can I Contact for Help?

Raise a ticket at the **Achronix Support Portal**[17].

15 https://www.achronix.com/documentation/ace-installation-and-licensing-guide-ug002
16 https://www.achronix.com/documentation/snapshot-user-guide-ug016
17 https://support.achronix.com/hc/en-us

> **Note**
>
> Entering a ticket require a support account. For details on how to register for a support account, visit **How Do I Register for an Achronix Support Account?**[18]

not

18 https://support.achronix.com/hc/en-us/articles/4404014677268-How-Do-I-Register-for-an-Achronix-Support-Account

Chapter 7 : Getting Started Guide Revision History

Version	Date	Description
1.0	26 Jan 2022	• Initial Achronix release.
1.1	19 Jul 2022	• Updated terminology: the I/O ring holds the various interface subsystems. • Added instructions on creating the interface subsystems used in the Quickstart design. • The Device Speed option C3 is being deprecated and replaced by C3L.
1.2	13 Oct 2023	• Remove references to end-of-life devices.
1.3	03 Dec 2024	• Updated Synplify Pro environment configuration. • Other minor edits and corrections.