Speedster7t DDR User Guide (UG096)

Speedster FPGAs

Achronix
Data Acceleration

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Chapter 1 : Introduction

The Achronix Speedster7t FPGA family provides DDR subsystems that enable the user to fully utilize the low latency and high-bandwidth efficiency of these interfaces for critical applications such as high-performance compute and machine learning systems. The number of DDR subsystems varies within the Speedster7t device family. The DDR subsystem supports memory devices and features compliant with JEDEC Standard JESD79-4B.

The AC7t1400/AC7t1500 FPGA contains a single high-speed DDR4 interface which can be used to connect to off-chip DDR4 memory devices, including a variety of dual in-line memory modules (DIMM) and memory components. The DDR4 controller IP in Speedster7t devices provides a low-power, low-latency and high-performance interface solution for external DDR4 SDRAM devices. The memory controller core clock runs at a maximum of 800 MHz to support data rates up to 3.2 Gbps per lane, which is achieved when the SDRAM clock operates at 1.6 GHz. The controller supports up to 72 bits of data including 8 bits of error correction code (ECC). The DDR4 controller and PHY in the subsystem are implemented as hard IP blocks inside the I/O ring of the AC7t1400/AC7t1500 FPGA.

The AC7t800 FPGA contains a single high-speed DDR4/5 interface which can be used to connect to off-chip DDR5 and DDR4 memory devices, including a variety of dual in-line memory modules (DIMM) and memory components. When making use of DDR5, the interface supports two channels. The memory controller core clock runs at a maximum of 1.4 GHz to support data rates up to 5.6 Gbps per lane (DDR5), which is achieved when the SDRAM clock operates at 2.8 GHz. The controller supports up to 80 bits of data including 16 bits of error correction code (ECC). The DDR controller and PHY in the subsystem are implemented as hard IP blocks inside the I/O ring of the AC7t800 FPGA.

DDR4 Feature Highlights

- **Data Rate** – Supports a data transfer rate per pin of up to 3200 Mbps, providing up to 25.6 GBps of memory bandwidth per chip.
- **Interface Width** – Up to 72-bit wide interface; data path width of 64 is supported. There are 8 check bits to support ECC, 1 bit per DQ byte.
- **Memory Density** – Supports memory densities that are compliant with JEDEC Standard JESD79-4B .
- **Memory Type** – Component mode, SODIMM, UDIMM, RDIMM, and LRDIMM.
- **Multi Rank** – Supports single-, dual- and quad-rank memories.
- **Data Bit Width** – ×4, ×8 and ×16 configuration supported.
- **DQ Format** – Double data rate; data latches on the rising and falling edge of the data strobe.
- **Banks** – Four bank groups in the DDR4 SDRAM, providing 16 internal banks that aid faster burst accesses.
- **Burst Modes** – Supports sequential BL8 burst mode and burst chop. Also supports partial reads and writes.
- **DQ Bus** – POD12 configuration that reduces I/O noise and power.
- **Data Mask and Data Bus Inversion** – Supports data mask and data bus inversion.
- **Low-Power Modes** – Supports self-refresh and low-power modes.
- **PHY Bypass Mode** – The user has the option to bypass the DDR4 PHY and utilize the associated DDR I/O pins for driving other interfaces. If the user does not require all 72 bits of the data bus, the unused byte lanes can also be bypassed to leverage the use of the designated I/O for other purposes.

- **Controller Bypass Mode** - Speedster AC7t1400/AC7t1500 devices do not support controller bypass or PHY-only mode.

DDR5 Feature Highlights

- **Data Rate** – Supports a data transfer rate per pin of up to 5600 Mbps, providing up to 44.8 GBps of memory bandwidth per device.
- **Interface Width** – Up to 80-bit wide interface; data path width of 64 is supported. Up to two channels are supported. There are 16 check bits to support ECC, 8 bits per channel.
- **Memory Density** – Supports memory densities that are compliant with JEDEC Standard JESD79-5A .
- **Memory Type** – Component mode: UDIMM and RDIMM.
- **Multi Rank** – Supports single-, dual- and quad-rank memories.
- **Data Bit Width** – ×4, ×8 and ×16 configuration supported.
- **DQ format** – Double data rate; data latches on the rising and falling edge of the data strobe.
- **Banks** – Four bank groups in the DDR5 SDRAM, providing 16 internal banks that aid faster burst accesses.
- **Burst Modes** – Supports sequential BL8, BL16 burst mode, and burst chop. Also supports partial reads and writes.
- **DQ Bus** – POD12 configuration that reduces I/O noise and power.
- **Data Mask and Data Bus Inversion** – Supports data mask and data bus inversion.
- **Low-Power Modes** – Supports self-refresh and low-power modes.
- **PHY Bypass Mode** – The user has the option to bypass the DDR PHY and utilize the associated DDR I/O pins for driving other interfaces. If the user does not require all 80 bits of the data bus, the unused byte lanes can also be bypassed to leverage the use of the designated I/O for other purposes.
- **Controller Bypass Mode**- Speedster AC7t800 DDR5 IP does not support controller bypass or PHY only mode.

> **Note**
>
> Data mask and data bus inversion modes and lower power modes can be controlled by the user via APB interface. For more details, contact Achronix.

Chapter 2 : Architecture Overview

AC7t1400/AC7t1500

The figure below shows the architecture of AC7t1400/AC7t1500 FPGA. The DDR4 memory interface resides on the south edge of the device. There are integrated PLLs in each of the four corners of the device that supply the external reference clocks to all high-speed peripheral interfaces.

The DDR4 subsystem can access the FPGA core logic in the following two ways:

- NoC interface – By accessing the NoC that allows high-speed data to flow between the FPGA fabric and high-speed interfaces. For details, refer to the **Speedster7t Network on Chip User Guide**[1] (UG089).
- Direct Connect interface – By using the direct fabric connection where the memory controller can be connected directly to the FPGA fabric, similar to existing (or traditional) solutions.

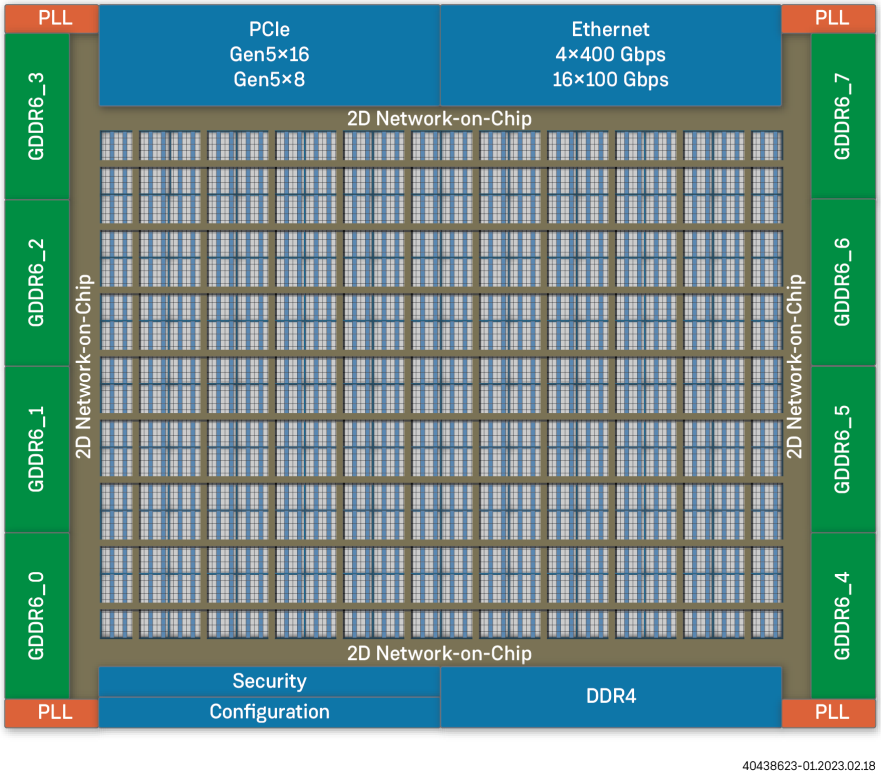

Figure 1 • Speedster7t Architecture Overview of DDR4 Interface

1 https://www.achronix.com/sites/default/files/docs/Speedster7t_2D_Network_on_Chip_User_Guide_UG089.pdf

AC7t800

The figure below shows the architecture of 7t800 FPGA. The DDR4/5 memory interface resides on the south edge of the device. There are integrated PLLs on the west side of the device that supply the external reference clocks to all high-speed peripheral interfaces.

The DDR4/5 subsystem can only access the FPGA core logic via NoC interface. For details, refer to the **Speedster7t Network on Chip User Guide**[2] **(UG089)**[3].

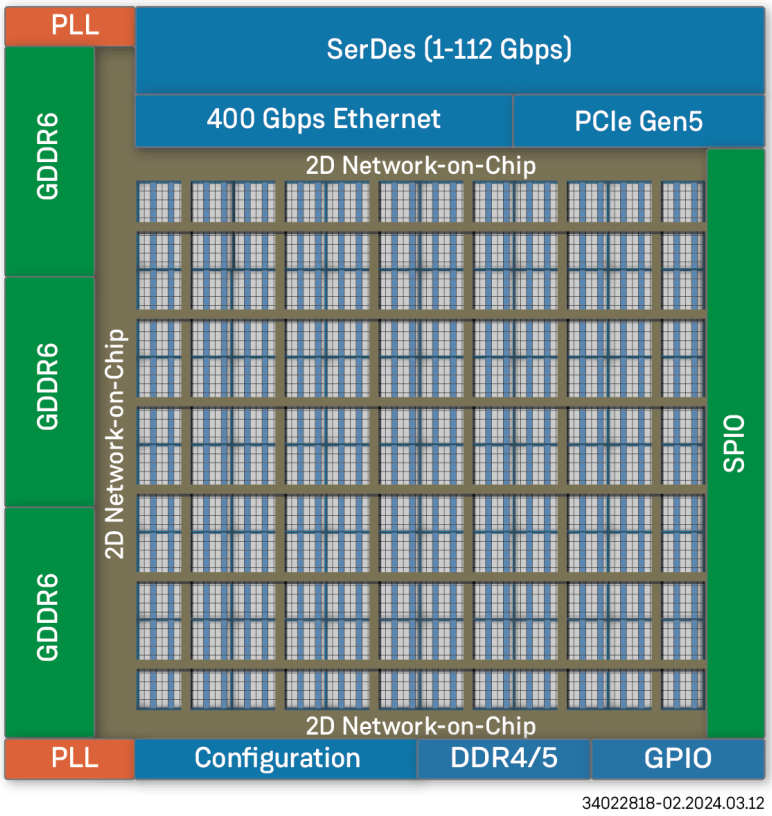

Figure 2 • Speedster7t Architecture Overview of DDR4/5 Interface

DDR4 Subsystem Overview

A DDR4 subsystem consists of a DDR4 controller, a PHY, a clock and reset block, and an APB interface that updates the control and status (CSR) registers, plus an AXI4 interface to connect to the user logic through either the NoC interface or directly on the FPGA fabric.

2 https://www.achronix.com/documentation/speedster7t-2d-network-chip-user-guide-ug089
3 https://www.achronix.com/documentation/speedster7t-2d-network-chip-user-guide-ug089

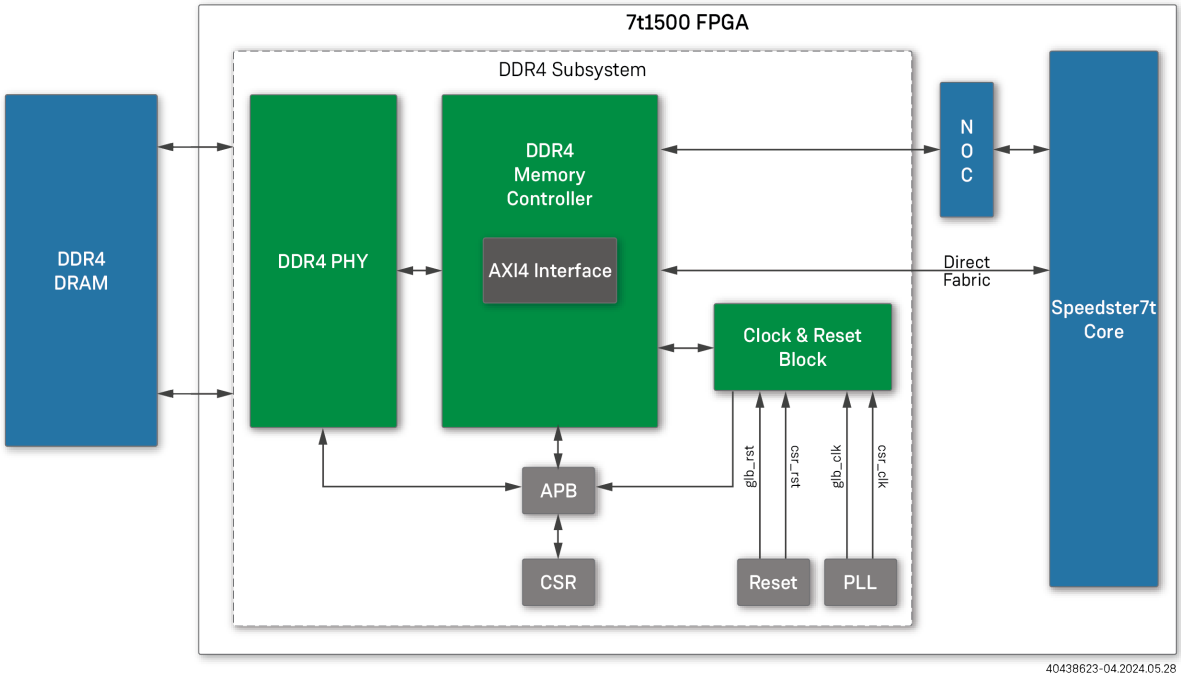

Figure 3 • DDR4 Subsystem Block Diagram

The following are key components that are required for a DDR4 memory interface operation:

Clock and Reset

The Speedster7t device has PLLs integrated in the four corners of the FPGA. The PLLs receive external reference clock inputs and generate global clocks used to drive the high-speed interfaces. The DDR4 PHY has an internal PLL that generates the memory clock used at the interface (for DQ/DQS/CA). When the DDR PHY clock runs at 800 MHz, the DDR4 DRAM clock operates at a maximum frequency of 1.6 GHz, generating data transactions at the maximum DDR4 data rate of 3.2 Gbps. The DDR4 memory uses a DDR protocol where data is latched at the rising and the falling edges of the data strobe. The reset circuitry generates global resets and at reset, the controller performs the required initialization of the external DDR4 memory, including calibration and programming of the internal mode registers.

DDR4 Controller

The DDR4 controller has a single clock input, usually driven by the device PLLs and and runs at a maximum frequency of 800 MHz. The read and write leveling operations are performed that match the PHY to the byte lane delays of the DIMM module.

- **Memory Read** – To perform a read, a user design signals a read request via the NoC or fabric logic, together with an address and data burst size. The controller responds with an acknowledgement before the data is made available. The controller then translates such a burst of data into multiple consecutive transactions.

- **Memory Write** – To perform a write, a user design signals a write request via the NoC or fabric logic, together with an address and burst size. When the DDR4 memory is ready to receive the data, the controller generates a data request that is sent to the PHY and the transaction is terminated when the data is written to the memory.
- **AXI4 Slave Interface** – The AXI4 slave interface in used in the memory subsystem to connect the controller to the FPGA fabric. This interface has two components: the AXI4 256-bit interface that talks to NoC interface and the AXI4 512-bit interface that connects the signals from controller directly to the user logic in the core through the direct-to-fabric interface.

DDR4 PHY

The DDR4 PHY enables the communication between the integrated memory controller and the external DDR4 memory. The PHY supports data width of 64 bits and speeds up to 3.2 Gbps per pin, delivering a maximum bandwidth of up to 25.6 GBps for a single-rank DIMM.

DDR4 DRAM Interface

The DDR4 PHY and the controller IP manages the memory transactions such as precharges, activates and refreshes. The controller issues commands as efficiently as possible, subject to the timing requirements of the DDR4 memory to achieve maximum efficiency

APB Interface

The APB interface operates at 250 MHz and enables the user to configure the DDR4 subsystem registers. The APB interface can be controlled either by the FPGA configuration unit (FCU), or from the fabric when the FPGA is in user mode. During device power-up, initialization, and bitstream loading, the FCU will configure many of the DDR4 subsystem registers. The user design may subsequently reprogram further registers as part of DDR4 calibration and training (with FPGA in user mode).

Achronix Device Manager Training

DDR4 interface initialization and training is performed by the Achronix Device Manager (ADM). For more information, refer to the **Soft IP User Guide**[4].

DDR4/5 Subsystem Overview

A DDR4/5 subsystem consists of a DDR4/5 controller, a PHY, a clock and reset block, and an APB interface that updates the control and status (CSR) registers, plus an AXI4 interface to connect to the user logic through the NoC interface.

4 https://www.achronix.com/sites/default/files/docs/Speedster7t_Soft_IP_User_Guide_UG103_3.pdf

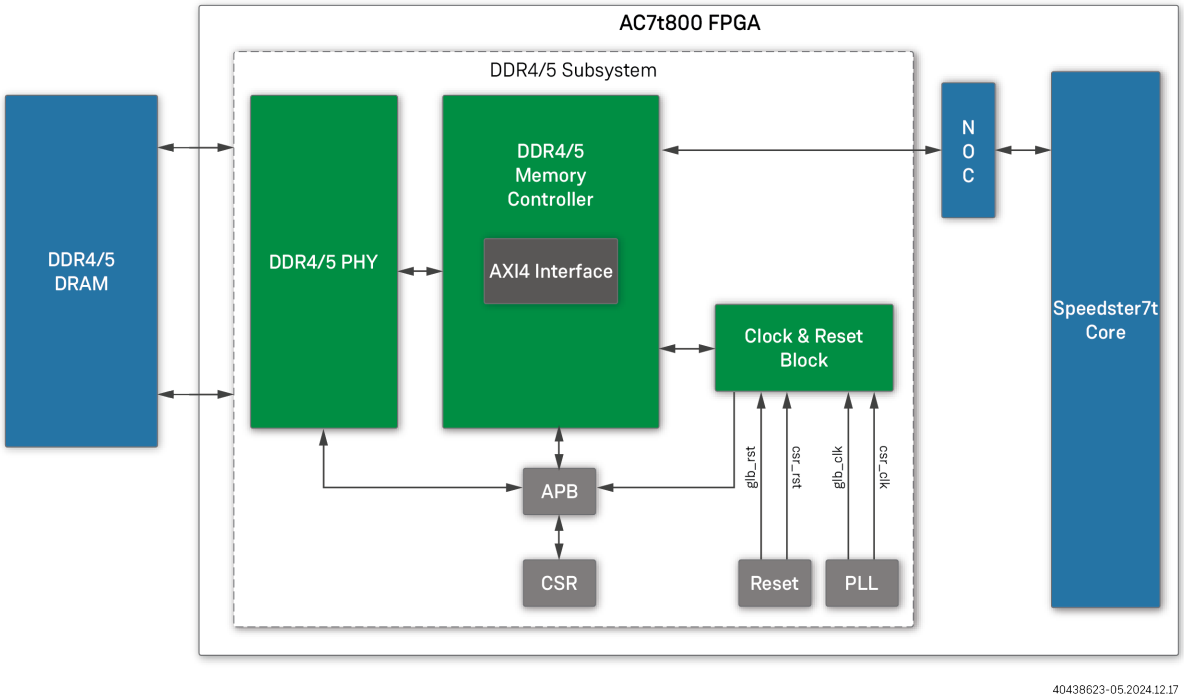

Figure 4 • DDR4/5 Subsystem Block Diagram

> **Note**
>
> This diagram represents a single channel on the DDR5 interface.

The following are key components that are required for a DDR4/5 memory interface operation:

Clock and Reset

The AC7t800 device has PLLs integrated in two corners of the FPGA. The PLLs receive external reference clock inputs and generate global clocks used to drive the high-speed interfaces. The DDR5 PHY has an internal PLL that generates the memory clock used at the interface (for DQ/DQS/CA). When the DDR PHY clock runs at 1400 MHz, the DDR5 DRAM clock operates at a maximum frequency of 2.8 GHz, generating data transactions at the maximum DDR5 data rate of 5.6 Gbps. The DDR5 memory uses a DDR5 protocol where data is latched at the rising and the falling edges of the data strobe. The reset circuitry generates global resets and at reset, the controller performs the required initialization of the external DDR5 memory, including calibration and programming of the internal mode registers.

DDR5 Controller

The DDR5 controller has a single clock input, usually driven by the device PLLs and and runs at a maximum frequency of 1400 MHz. The read and write leveling operations are performed that match the PHY to the byte lane delays of the DIMM module.

- **Memory Read** – To perform a read, a user design signals a read request via the NoC, together with an address and data burst size. The controller responds with an acknowledgement before the data is made available. The controller then translates such a burst of data into multiple consecutive transactions.
- **Memory Write** – To perform a write, a user design signals a write request via the NoC, together with an address and burst size. When the DDR5 memory is ready to receive the data, the controller generates a data request that is sent to the PHY and the transaction is terminated when the data is written to the memory.
- **AXI4 Slave Interface** – The AXI4 slave interface in used in the memory subsystem to connect the controller to the FPGA fabric. This interface has the AXI4 256-bit interface that talks to NoC interface.

DDR5 PHY

The DDR5 PHY enables the communication between the integrated memory controller and the external DDR5 memory. The PHY supports data width of 80 bits and speeds up to 5.6 Gbps per pin, delivering a maximum bandwidth of 44.8 GBps for a single-rank DIMM.

DDR5 DRAM Interface

The DDR5 PHY and the controller IP manages the memory transactions such as precharges, activates and refreshes. The controller issues commands as efficiently as possible, subject to the timing requirements of the DDR5 memory to achieve maximum efficiency

APB Interface

The APB interface operates at 250 MHz and enables the user to configure the DDR5 subsystem registers. The APB interface can be controlled either by the FPGA configuration unit (FCU), or from the fabric when the FPGA is in user mode. During device power-up, initialization, and bitstream loading, the FCU will configure many of the DDR5 subsystem registers. The user design may subsequently reprogram further registers as part of DDR5 calibration and training with FPGA in user mode.

Achronix Device Management Training

DDR5 interface initialization and training is performed by the Achronix Device Management system. This module is located within the I/O ring that runs on a 250 MHz reference clock. Further details on how to configure this module can be found in the chapter, "**DDR IP Software Representation in ACE (page 44)**".

Users will also need to set up this reference clock in ACE. Details on how to configure the clock accordingly can be found in the ***Speedster7t Clock and Reset Architecture User Guide*** **(UG083)**[5].

> ⓘ DDR4 operates the same as AC7t1500.

Bypass Mode

The bypass mode in the DDR4/5 subsystem is provided to enable fully independent control of the DDR4/5 I/O from user implemented logic through the fabric. It is mainly used in test/debug environment.

5 https://www.achronix.com/documentation/speedster7t-clock-and-reset-architecture-user-guide-ug083

In bypass mode, the DDR4/5 controller and PHY are completely bypassed. The DDR4/5 input and output pins are directly connected to the core fabric in this mode. These pins are only suitable for low speed asynchronous applications, running at a maximum frequency of 100 MHz. Bypass mode is enabled when a user drives a logic 1 to the three bypass mode enable pins from the core fabric. More details can be seen in the **Bypass Interface**[6] section.

6 http://DDR NoC and Fabric Connectivity#BypassInterface

Chapter 3 : DDR Controller Architecture

The DDR controller IP in Speedster7t devices contains the logic necessary to accept read and write requests to off-chip DDR memory and translates these requests into command sequences. The memory controller ensures proper SDRAM initialization; performs address mapping from system addresses to SDRAM addresses with correct rank, bank group, bank addresses; accepts requests with system addresses and associated data for writes; prioritizes requests to minimize the latency of reads (especially high-priority reads); and maximize page hits. The controller also ensures that refresh functions and other memory and PHY maintenance requests are carried out as required. When the SDRAM enters and exits various power-saving modes, the controller ensures that these operations are executed appropriately.

DDR4 Controller Features

Here is a list of features that the DDR4 controller in AC7t1400/AC7t1500 device support:

Table 1 • DDR4 Controller Features

Feature	Description
Supported maximum data rate	Memory controller supports DDR4 operation at up to 204.8 (64 × 3.2) Gbps per channel
Controller clock rate	Runs at a clock rate of 800 MHz to support maximum data rate 3.2 Gbps
Memory protocol	DDR4
Memory type	Component mode, UDIMM, RDIMM, LRDIMM, SODIMM; No 3DS support;
Memory configurations	Supports ×4, ×8 and ×16 bit-width configurations
Number of channels	Supports single-channel mode with 72 data bits
Burst modes	• BL8 • Burst chop
Data bus width mode	Supports full, half and quarter bus width modes
Multi ranks	Supports up to four physical ranks

Feature	Description
Power saving	• Clock gating • Self refresh • Dynamic tri-stating • Low-power modes
Refresh control	• Supports per bank and all bank refresh • Automatic refresh
Data mask (DM) and data bus inversion (DBI)	Supports data masking and data bus inversion
Page policy	• Per command auto-precharge control • Open-page
Memory error correcting code	Supports ECC
Command address parity	Supports command address parity
ZQ control	Automatic ZQ command enable/disable
DDR4-specific features	• On-die termination • CA parity (except retry feature) • Power-down auto-precharge (PDA) • Programmable preamble (2tCK)

Table Note

This table is also applicable to AC7t800 if implementing DDR4.

DDR5 Controller Features

The table below lists the features that the DDR5 controller in AC7t800 devices support:

Table 2 • DDR5 Controller Features

Feature	Description
Supported maximum data rate	Memory controller supports DDR5 operation at up to 448 (80 × 5.6) Gbps per channel

Feature	Description
Controller clock rate	Runs at a clock rate of 1400 MHz to support maximum data rate 5.6 Gbps
Memory protocol	DDR5 ▪ Two independent controller channels ▪ Programmable Channel interleaving ▪ CA parity, write/read CRC ▪ On-chip parity ▪ Multi- and single-beat ECC
Memory type	Component mode: UDIMM, RDIMM
Memory configurations	Supports ×4, ×8 and ×16 bit-width configurations
Number of channels	Supports dual-channel mode with 80 data bits
Burst modes	· BL16 · OTF burst · Burst chop
Data bus width mode	Supports full bus width mode
Multi ranks	Supports up to four physical ranks
Power saving	· Clock gating · Self refresh · AXI/DDRC low-power modes · Dynamic tri-stating
Refresh control	· Supports per-bank and all-bank refresh · Automatic refresh
Data mask (DM) and data bus inversion (DBI)	Supports data masking and data bus inversion
Page policy	· Per command auto-precharge control · Open-page · Close-page
Memory error correcting code	Supports ECC

Feature	Description
Command address parity	Supports command address parity
ZQ control	Automatic ZQ command enable/disable
DDR5-specific features	• On-die termination • 2D read and write training • CA parity (except retry feature) • Power-down auto-precharge (PDA) • Programmable preamble (2tCK)

Controller Architecture Overview

AC7t1400/AC7t1500

The figure below gives an overview of the DDR4 memory controller IP on the AC7t1400/AC7t1500 devices and shows its sub blocks, the controller core, port arbiter, AXI port interface, SRAM memories to implement the read reorder buffer (RRB), write-data RAM and the APB Interface.

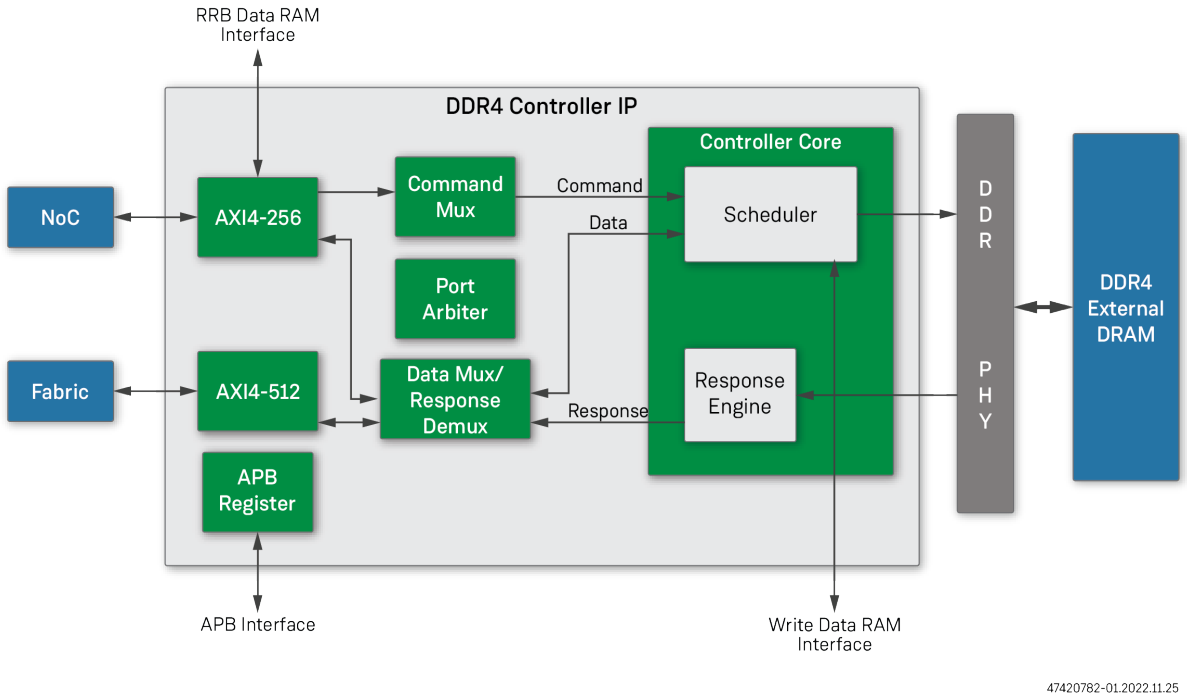

Figure 5 • DDR4 Memory Controller Block Diagram

AC7t800

The figure below gives an overview of the DDR5 memory controller IP on the AC7800 devices and shows its sub blocks, the controller core, port arbiter, 2x256 NoC AXI port interface, SRAM memories to implement the read reorder buffer (RRB), write-data RAM and the APB Interface.

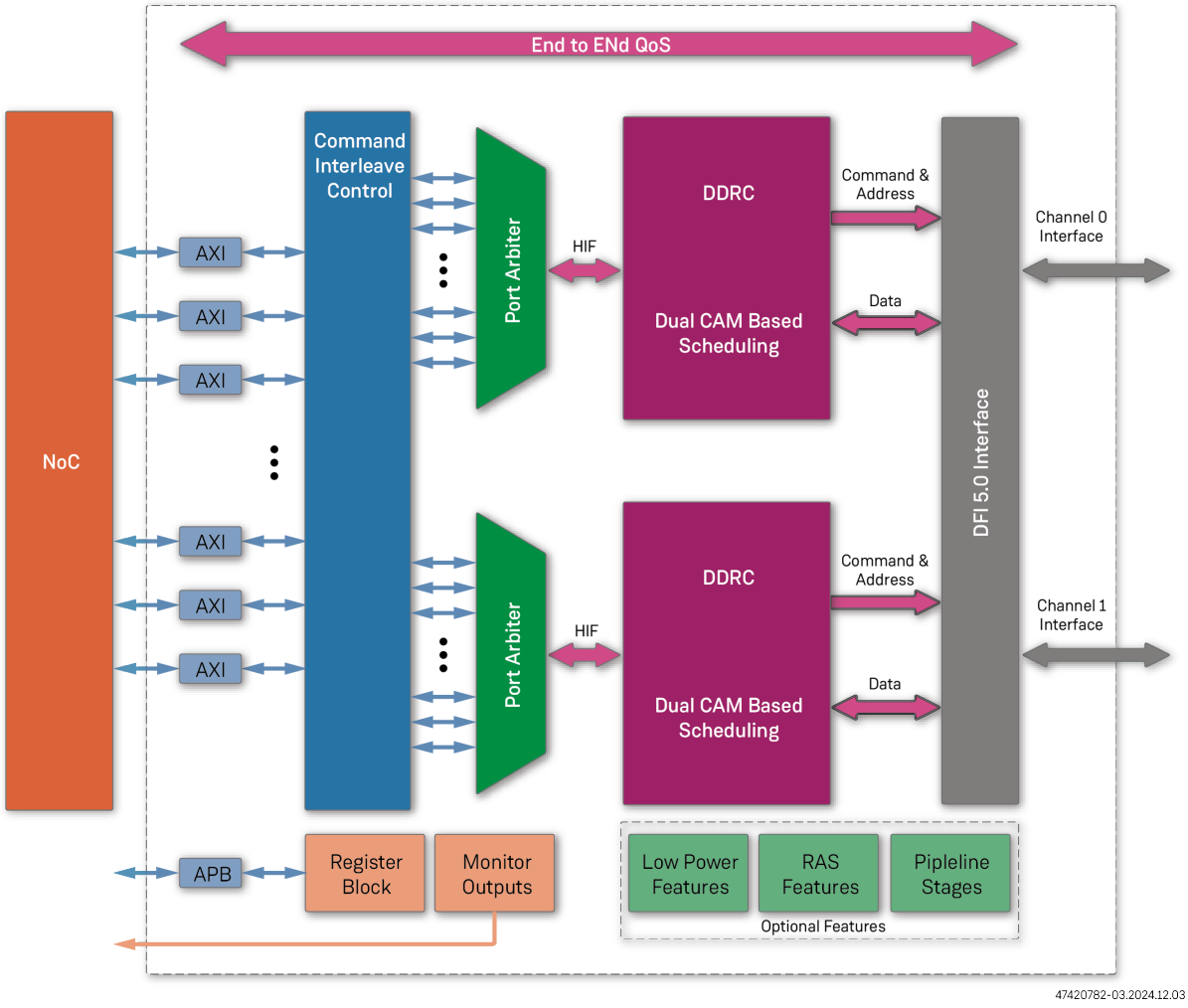

Figure 6 • DDR5 Memory Controller Block Diagram

Controller Components Overview

The DDR memory controller IP across all Speedster7t devices contains the following main architectural blocks.

Port Arbiter (PA) Block

This block provides latency-sensitive, priority-based arbitration between the addresses issued by the AXI ports for command requests from AXI ports to the DDR controller.

Controller Core

This block contains a logical content-addressable memory (CAM), that holds information on the commands, that is used by the scheduling algorithms to optimally schedule commands to be sent to the PHY, based on priority, bank/rank status and DDR timing constraints. The write data is stored in an embedded SRAM internal and external to the controller until its associated command is issued to the DDR4 PHY. The read data is handled by the response engine in the controller core and is returned in the order of scheduled read commands on the host interface. ECC handling is an optional function, which is handled by logic modules within the controller core in the write data path and in the response engine.

RAM Interfaces

The memory controller implements a read reorder buffer so that the read data can be returned from the controller core in a different order from which the read commands are forwarded from the AXI interface. This reordering of read commands in the controller helps maximize DRAM bandwidth. There is also a write-data RAM for storing data until the time the data can be made available to the controller core.

AXI4 Slave Interface

The AXI transactions are input to the controller through the NoC interface via the 256-bit AXI4 interface or directly to an adjacent fabric cluster using the 512-bit AXI4 interface. The AXI clocks for the NoC and direct connections (to the fabric) are asynchronous to each other. The resets for these AXI interfaces, are synchronized for de-assertion with their respective AXI clocks before they are input to the memory controller.

This burst-based interface enables read and write request channels that specify the host ID for the request, start byte address, burst length, burst size, and burst type. This information is processed by the interface and is used subsequently by the DDR controller core. The AXI ports interface with the controller core to perform read/write address and data/response generation. Read data is stored in a buffer and returned in order to the AXI ports.

APB Interface

The APB interface is used to configure the clocks and resets in the DDR subsystem. The APB interface also makes the internal registers of both the controller and the PHY accessible to the user logic. The APB interface to the DDR subsystem consists of a 28-bit address and a 32-bit data bus. The subsystem control and status registers address (CSR) and memory controller address are used as-is from the APB interface. The available configuration space through the APB bus to which the memory controller is mapped is in the address range 0x000_0000 to 0xFFF_FFFF.

The table below describes the configuration space register address allocation for the controller, PHY and the DDR subsystem.

> **note**
>
> A detailed description of these register bits will be provided in a future release of this guide.

Table 3 • Control and Status Register Address Map

Address Range	Accessible Space
0x000_0000 to 0x0FF_FFFF	Memory controller register space
0x100_0000 to 0x1FF_FFFF	PHY register space and PHY training FW memory access
0x200_0000 to 0x2FF_FFFF	Subsystem control and status register space

Chapter 4 : DDR PHY Architecture

PHY Overview

The embedded Speedster7t DDR PHY supports the DDR memory standard at the channel interface and the DFI-4.0 interface on the FPGA side with the memory controller.

The figure below shows the PHY interfacing with the off-chip DDR memory on one side and the embedded DDR memory controller on the FPGA side.

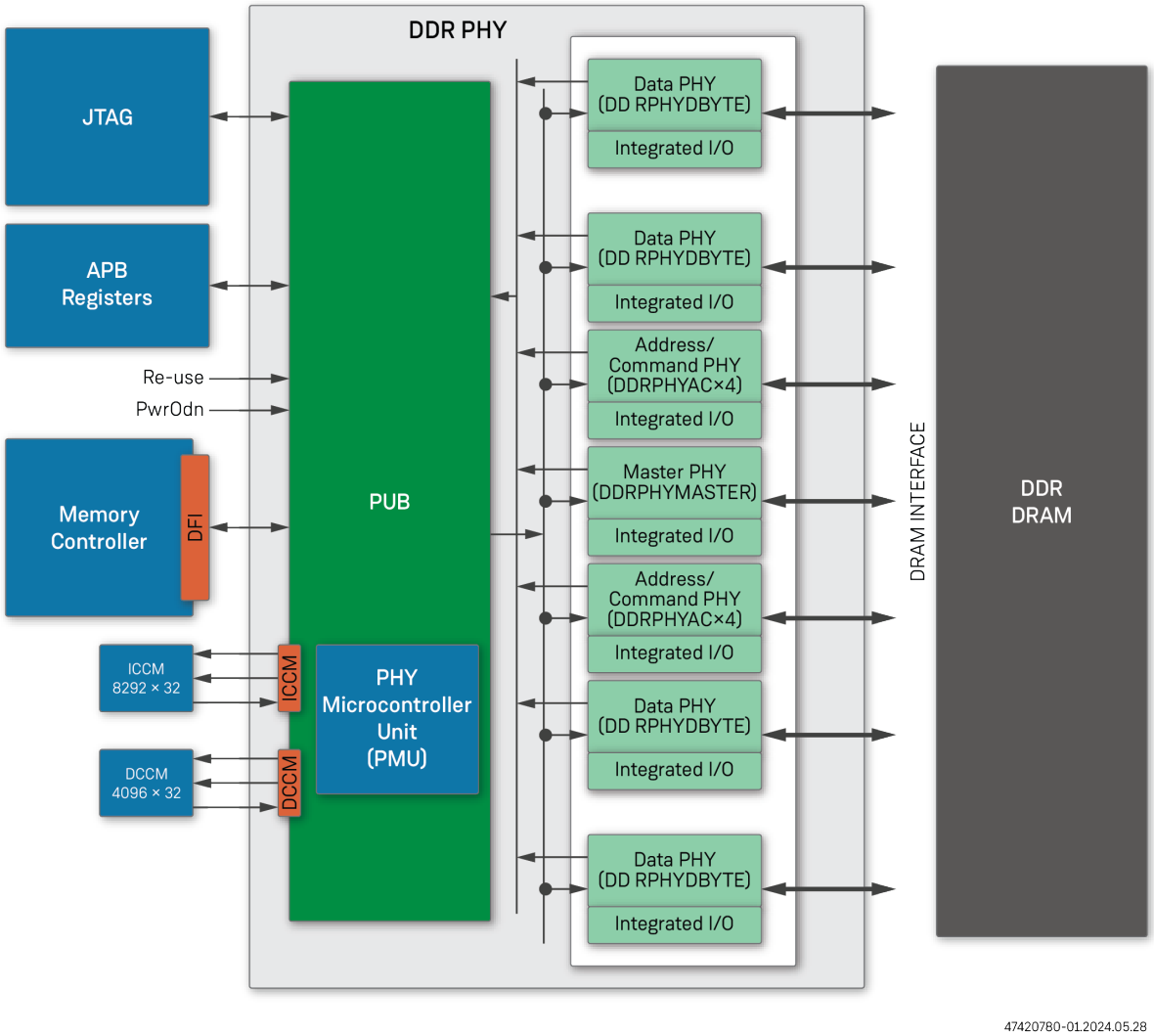

Figure 7 • DDR PHY Block Diagram

> **Note**
>
> For DDR4, Dbytes 0 to 7 will be connected to a single DIMM/component. For DDR5, Dbytes 0-3 will be connected to channel A and Dbytes 4-7 will be connected to channel B.

PHY Features

AC7t1400/AC7t1500 DDR4

Feature	Description
PHY rate	The PHY operating frequency is at a max of 800 MHz.
DRAM maximum data rate	High-performance DDR4 PHY supporting data rates up to 3.2 Gbps per data pin
Memory protocol	DDR4
Memory type	Component mode: UDIMM, RDIMM, LRDIMM, SODIMM
Memory configurations	Supports ×4, ×8 and ×16 bit width configurations
Number of channels	Supports single-channel mode with 64 data bits
Multi-rank support	Supports up to four physical ranks
Embedded DLLs	Voltage and temperature compensated delay lines used for DQS centering; DDR4 read/write leveling and per-bit deskew
Embedded PLL	Includes a low-jitter PLL for both PHY clock generation and SDRAM clock generation
Other DDR4 features	• DRAM addressing up to 16Gb • Supports data bus inversion (DBI) • Command address parity • Per DRAM addressability • Programmable input on-die termination (ODT) and output impedance • Programmable preamble (2tCK) (*check)

AC7t800 DDR5

Feature	Description
PHY rate	The PHY operating frequency is at a max of 1400 MHz.
DRAM maximum data rate	High-performance DDR4 PHY supporting data rates up to 5.6 Gbps per data pin
Memory protocol	DDR5
Memory type	Component mode: UDIMM, RDIMM
Memory configurations	Supports ×4, ×8 and ×16 bit width configurations
Number of channels	Supports dual-channel mode with 64 data bits
Multi-rank support	Supports up to four physical ranks
Embedded DLLs	Voltage and temperature compensated delay lines used for DQS centering; DDR5 read/write leveling and per-bit deskew
Embedded PLL	Includes a low-jitter PLL for both PHY clock generation and SDRAM clock generation
Other DDR5 features	• DRAM addressing up to 16Gb • Supports data bus inversion (DBI) • Command address parity • Per DRAM addressability • Programmable input on-die termination (ODT) and output impedance • Programmable preamble (2tCK) (*check)

PHY Architecture

The embedded DDR PHY IP in Speedster7t FPGAs consists of multiple components shown in the block diagram above. The sections that follow describe each of these components,

DDRPHYACX4

The DDRPHYACX4 is the PHY component for the address/command lane. Features of this component include:

- High-speed digital logic pipeline for transmitting address/command to the SDRAM.
- I/O component that includes PVT-compensated output impedance.

DDRPHYDBYTE

The DDRPHYDBYTE is the data receive/transmit building component for the DDR PHY, statically configurable as one byte-wide data lane. Features of the DDRPHYDBYTE include:

- High-speed digital logic pipeline for transmit and receive datapaths to and from the SDRAM.
- I/O component that includes PVT-compensated, on-die termination (ODT) and output impedance.

MASTER PHY

The master PHY is the location of the high-speed PLL used to generate the high-speed clock for data transmit and high-speed digital pipelines. The PLL has the following modes of operation:

- The PLL block generates the actual DRAM bit-rate clock.
- Power on reset (POR) circuit, I/O macros for DRAM reset, DRAM alert_n signals.

PHY Utility Block (PUB)

The PHY utility block provides configuration, control, and other utility functions for all PHY hard components. This block handles a variety of functions for the PHY, including driving initialization sequences, providing all training functions, implementing the DFI protocol, implementing registers and a register access bus.

ICCM and DCCM Memories

The microcontroller in the utility block, which runs the training firmware, requires two memories: DCCM and ICCM memories. These firmware memories are accessible on APB interface as a contiguous CSR space. The ICCM is mapped on PHY CSR address space to the address range 0x0005_0000 to 0x0005_7FFF. The DCCM is mapped on PHY CSR address space to the address range 0x0005_4000 to 0x0005_3FFF . These memories are loaded during bitstream configuration via APB bus and are both word addressable.

PHY Clocking

One of the global clocks generated by the device PLLs is selected as the core clock that drives both the memory controller core and the PHY. The PHY clock operates at a maximum of 800 MHz for DDR4 and 1400 MHz for DDR5 and is required to be synchronous to the controller core clock. This PHY clock generates the external DDR SDRAM memory clock at 1.6 GHz that helps achieve the data rate of 3.2 Gbps on the memory interface on DDR4. This PHY clock generates the external DDR SDRAM memory clock at 2.8 GHz that helps achieve the data rate of 5.6 Gbps on the memory interface on DDR5.

Chapter 5 : DDR Clock and Reset Architecture

A Speedster7t device requires external input reference clock and reset signals to drive the DDR memory interface. The Speedster7t device clock and reset generator module consists of PLLs, DLLs and reset circuitry to generate these signals. There is a clock and reset generator placed in each corner of the device on the AC7t1400/AC7t1500 and in each of the western corners on the AC7t800. Each clock and reset generator has four PLLs, with each PLL capable of generating up to four clock outputs, The subsystem can utilize global clocks chosen from two adjacent PLL's clock outputs. Refer to the **Speedster7t Clock and Reset Architecture User Guide[7] (UG083)**[8] for further details.

The DDR subsystem requires the following clocks selected from the global clock network. These clocks can be sourced from either a single or multiple PLLs. The DDR subsystem requires the following clocks:

- DDR memory controller and PHY reference clock
- Input reference clock for the 256-bit AXI4 NoC interface
- Input reference clock for the 512-bit direct-to-fabric-connect AXI4 interface (only applicable to DDR4 on AC7t1400/AC7t1500)

Similarly, there are 32 global resets generated by the clock and reset generators. In addition, there are an additional 48 active-low resets. Any of these resets can be selected to provide the reset input to the DDR subsystem. Alternatively, the DDR subsystem reset source can be driven by the FCU.

The diagram below depicts the flow of all the clocks and resets required for the DDR4 subsystem on AC7t1400/AC7t1500.

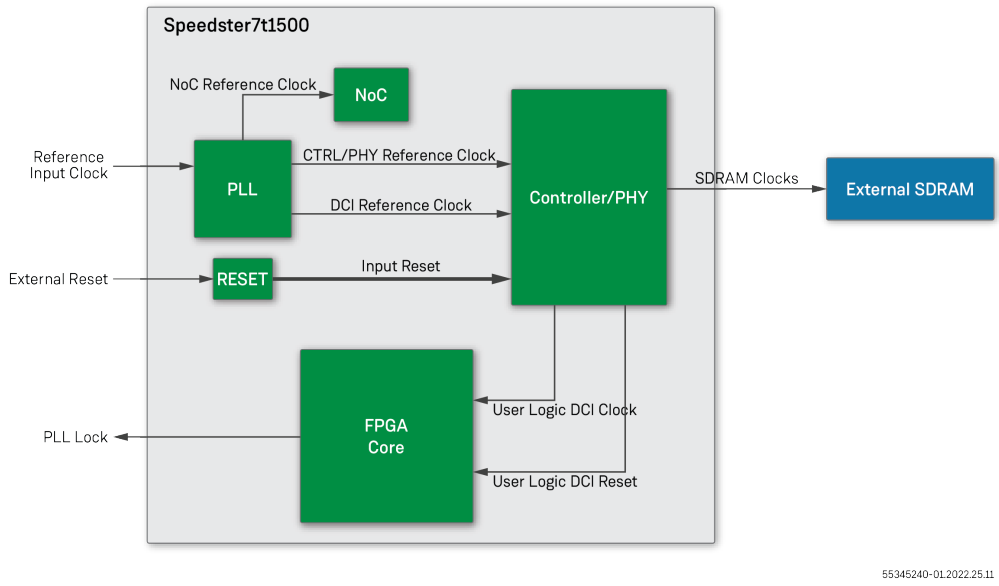

Figure 8 • Clock and Reset Architecture of DDR4 Subsystem on AC7t1400/AC7t1500

7 https://www.achronix.com/documentation/speedster7t-clock-and-reset-architecture-user-guide-ug083
8 https://www.achronix.com/documentation/speedster7t-clock-and-reset-architecture-user-guide-ug083

The diagram below depicts the flow of all the clocks and resets required for the DDR5 subsystem on AC7t800.

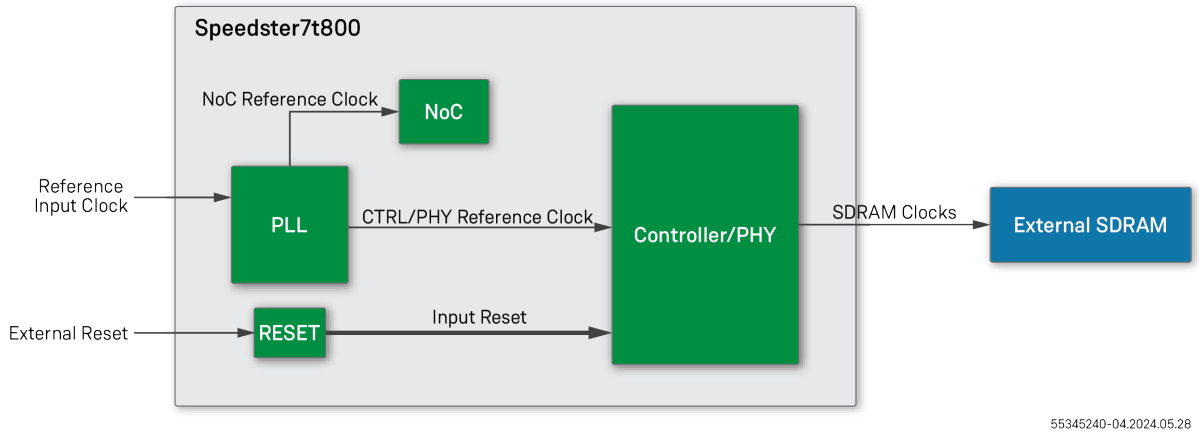

Figure 9 • Clock and Reset Architecture of DDR5 Subsystem on AC7t800

DDR4 Subsystem Clocks

The DDR4 memory controller clock is selected from one of the global clocks generated by the PLL and runs at a maximum of 800 MHz to support maximum data rate of 3200 Mbps (achieved when DDR4 SDRAM memory clock runs at 1600 MHz). The DDR4 PHY clock is also selected from the same clock source as the controller clock. The PHY's internal PLL generates the external SDRAM memory clock. When the PHY runs at 800 MHz, the DDR4 memory operates at the maximum supported data rate.

The AXI4 interface requires two asynchronous clocks selected separately by the user in ACE I/O designer. These clocks drive the 256-bit AXI4 interface connected to the peripheral NoC and the 512-bit AXI4 interface connected to the fabric. The NoC reference input clock always operates at 200 Mhz and is selected from the global clock outputs. The clock driving the DDR user logic for the NoC interface is handled internally in the NoC. The direct-to-fabric connection (DC) AXI clock, also chosen from a global clock drives the DDR user logic for the DC interface. The NoC and DC interface reference input clock rates are independent of the controller/PHY clock rate; users can scale these clocks based on their throughput requirements.

Both the AXI interface clocks are routed through the DDR subsystem and then fed to the NoC or the DC interface for driving user logic to avoid clock divergence issues. All clock domain crossings are also handled internally within the DDR4 subsystem.

The table below shows the maximum operating frequencies and the relationships between the different clock domains in the DDR4 subsystem. The user can scale the clocks maintaining the ratios and achieve desired rates of operation.

Table 4 • DDR4 Subsystem Clocks

DDR4 Data Rate	Controller Clock(1)	PHY Clock(1)	SDRAM Clock(2)
3200 Mbps	800 MHz	800 MHz	1600 MHz

DDR4 Data Rate	Controller Clock[1]	PHY Clock[1]	SDRAM Clock[2]
2666 Mbps	667 MHz	667 MHz	1333 MHz
2400 Mbps	600 MHz	600 MHz	1200 MHz

Table Notes

1. The controller and PHY clock always operate at half rate of the SDRAM clock.
2. The external SDRAM clock always operates at DATA_RATE/2 of the DDR4 memory. For example, if the DDR4 memory is operating at 3200 Mbps, memory clock frequency will be 1600 MHz.

DDR5 Subsystem Clocks

The DDR5 memory controller clock is selected from one of the global clocks generated by the PLL and runs at a maximum of 1400 MHz to support maximum data rate of 5600 Mbps (achieved when DDR4 SDRAM memory clock runs at 2800 MHz). The PHY's internal PLL generates the external SDRAM memory clock. When the PHY runs at 700 MHz, the DDR memory operates at the maximum supported data rate.

The AXI4 interface requires two asynchronous clocks selected separately by the user in ACE I/O designer. These clocks drive the 256-bit AXI4 interface connected to the peripheral NoC. The NoC reference input clock always operates at 200 Mhz and is selected from the global clock outputs. The clock driving the DDR user logic for the NoC interface is handled internally in the NoC. The NoCinterface reference input clock rates are independent of the controller/PHY clock rate; users can scale these clocks based on their throughput requirements.

Both the AXI interface clocks are routed through the DDR subsystem and then fed to the NoC to avoid clock divergence issues. All clock domain crossings are also handled internally within the DDR5 subsystem.

The table below shows the maximum operating frequencies and the relationships between the different clock domains in the DDR4 subsystem. The user can scale the clocks maintaining the ratios and achieve desired rates of operation.

Table 5 • DDR4 Subsystem Clocks

DDR4 Data Rate	Controller Clock	PHY Clock	SDRAM Clock[1]
5600 Mbps	700 MHz	1400 MHz	2800 MHz

Table Notes

1. The external SDRAM clock always operates at DATA_RATE/2 of the DDR4 memory. For example, if the DDR4 memory is operating at 3200 Mbps, memory clock frequency will be 1600 MHz.

DDR Subsystem Resets

The DDR subsystem has access to 80 available resets: 32 global resets and 48 active-low startup resets. The controller reset is asynchronous to the controller clock and is synchronized for de-assertion in the subsystem before it is sent to the memory controller. All resets can also be configured through IPCNTL reset selection registers.

> **Note**
>
> The details of these register settings to be programmed using the APB interface will be covered in future releases of the user guide.

When the user exercises the NoC interface, the NAPs require a reset input that can be driven from any of the available resets or generated by user logic. When the direct-to-fabric connect is utilized, the DDR4 subsystem outputs the reset to the FPGA fabric (DCI Reset as shown in the block diagram).

External Clock and PLL Connection

All the corner PLLs can be utilized to generate clocks for the DDR subsystem to perform at maximum data rates. The following figures illustrate how a user can connect the external reference input clock to drive the DDR4 subsystem. In the figure below, the south-west PLL generates clocks that drive the DDR subsystem clocks and the DDR interface SDRAM clock (ck_p and ck_n).

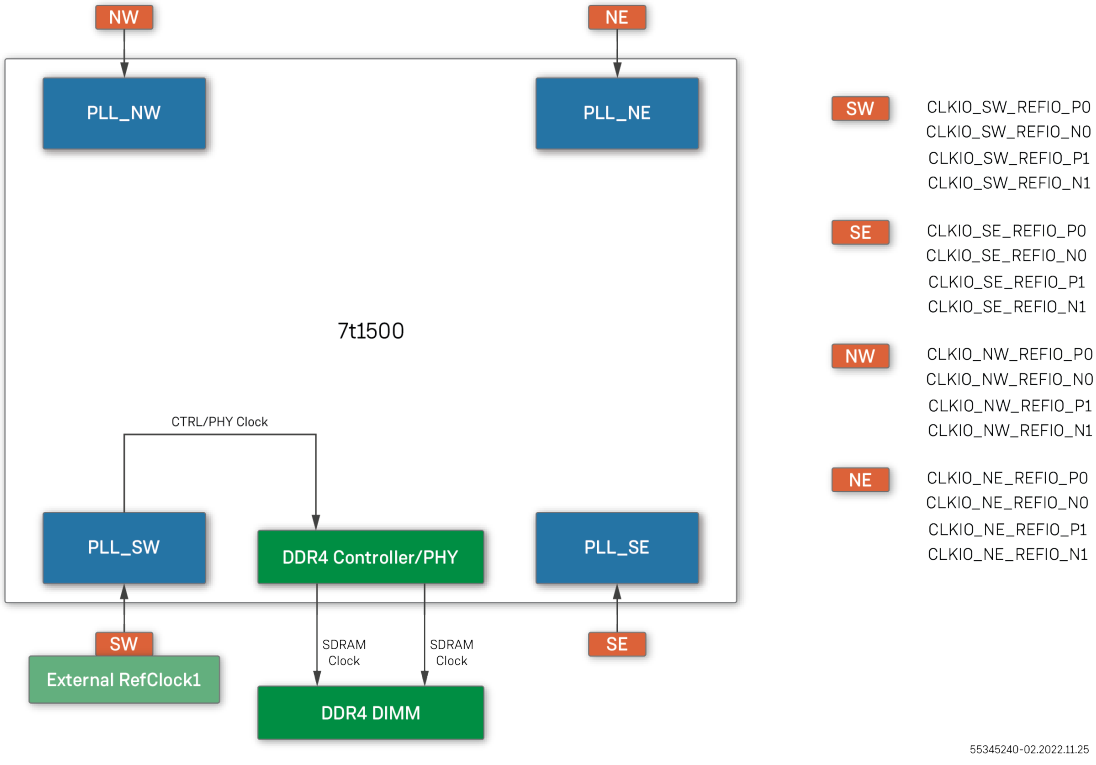

Figure 10 • South PLLs Driving the DDR Subsystem

> **Note**
>
> On AC7t800, the PLLs on the east side of the fabric are not available

The figure below shows the north-east PLL generates clocks that drive the north-west PLL which subsequently can be used to generate DDR clocks:

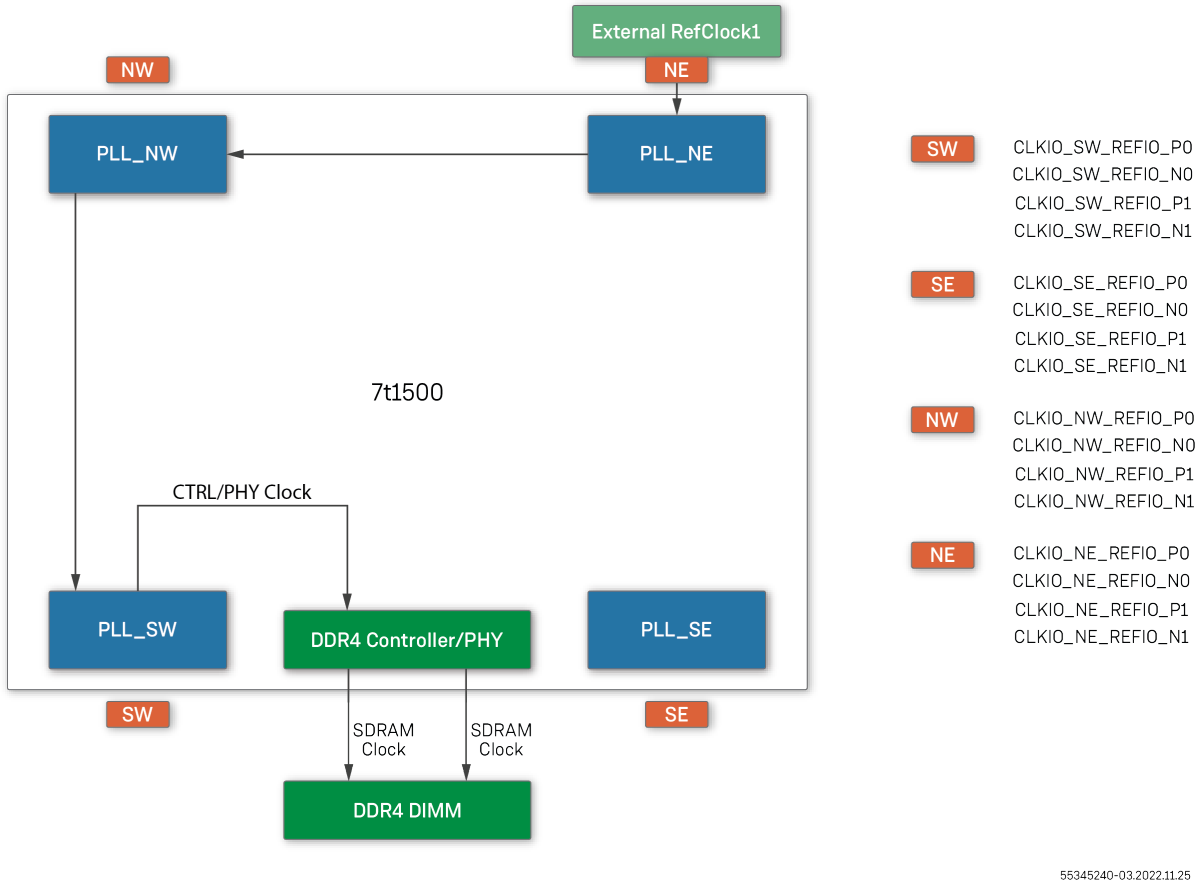

Figure 11 • North PLLs Driving the DDR Subsystem

> On AC7t800, the PLLs on the east side of the fabric are not available so the external reference clock would not come from PLL_NE

Chapter 6 : DDR NoC and Fabric Connectivity

The following sections describe the two interfaces supported by the DDR subsystem to connect to the user logic, namely the network on chip (NoC) and the direct connect (DC) interfaces. The DC interface can only be used on AC7t1400/AC7t1500. The DDR4 subsystem can also be configured to utilize both interfaces at the same time. If a transaction arrives on the NoC, the DDR subsystem will respond to it via the NoC interface. Similarly, if a transaction arrives on the DCI, the DDR subsystem will respond to it via the DCI. This capability is demonstrated in the DDR user reference design. Both NoC and DC interfaces use a standard AXI4 protocol; details of the specification can be found at **AXI Protocol Specification.**[9]

Connectivity to the NoC

The Speedster7t FPGA architecture has a network on chip that enables extremely high-speed data flow between the FPGA's core and its interfaces, as well as between logic within the FPGA fabric itself. The DDR subsystem can receive transactions initiated by the FPGA fabric or by PCIe via the NoC. For more details on the NoC, refer to the ***Speedster7t 2D Network on Chip User Guide*** **(UG089)**[10].

The NoC interface connectivity to the DDR subsystem is the default connection in ACE I/O Designer toolkit :

- This interface exists as part of the controller interface and the user does not need to create it.
- The user will need to only establish a connection from master logic in the fabric to the NoC by instantiating the ACX_NAP_AXI_SLAVE macro in the user design (refer to the section, ACX_NAP_AXI_SLAVE, in the **Speedster7t Component Library User Guide**[11] **(UG086)**[12]. Once a connection is established the master logic can send AXI transactions through the NoC interface to the DDR memory.
- For transactions from the PCIe subsystem via the NoC interface, the user needs to configure the PCIe subsystem, the NoC and the DDR4 subsystem in the I/O Designer Toolkit and requires the PCIe subsystem to send AXI commands to the DDR memory addresses.

The following figure shows how the master logic in the FPGA fabric sends and receives transactions from the DDR interface utilizing the NoC as seen on AC7t1400/AC7t1500.

9 https://developer.arm.com/docs/ihi0022/g
10 https://www.achronix.com/documentation/speedster7t-2d-network-chip-user-guide-ug089
11 https://www.achronix.com/documentation/speedster7t-component-library-user-guide-ug086
12 https://www.achronix.com/documentation/speedster7t-component-library-user-guide-ug086

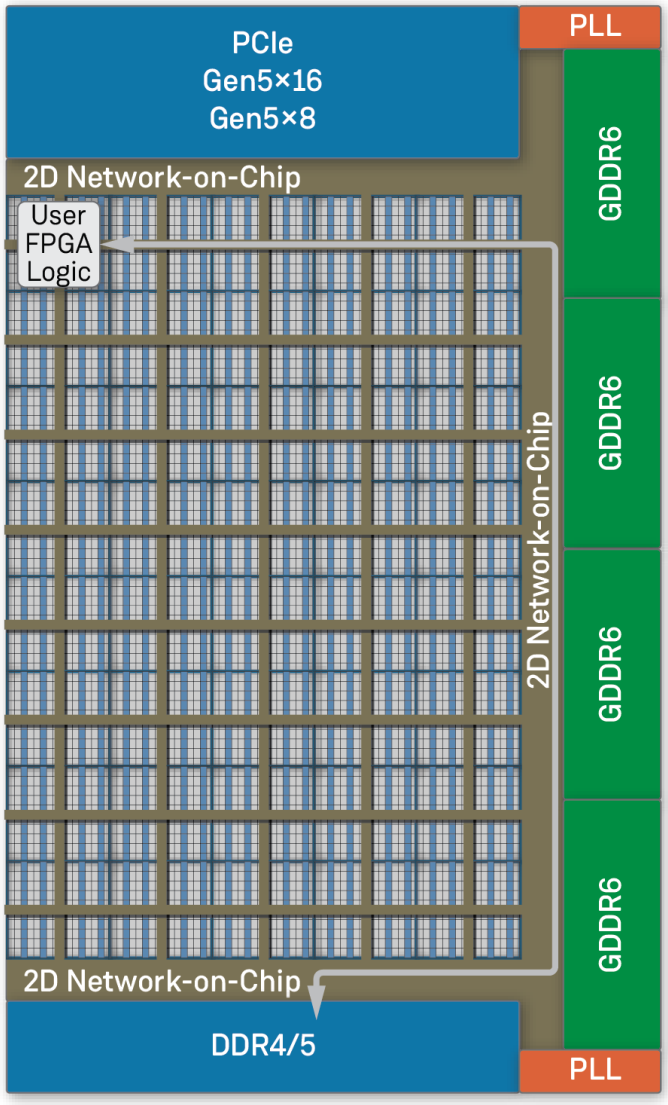

Figure 12 • Data Flow from Core Logic in FPGA Fabric to DDR4 Through the NoC as seen on AC7t1400/ AC7t1500

The figure below shows the PCI Express master issuing a transaction to the NoC, which is transmitted directly to the DDR4 interface without involving resources within the FPGA fabric.

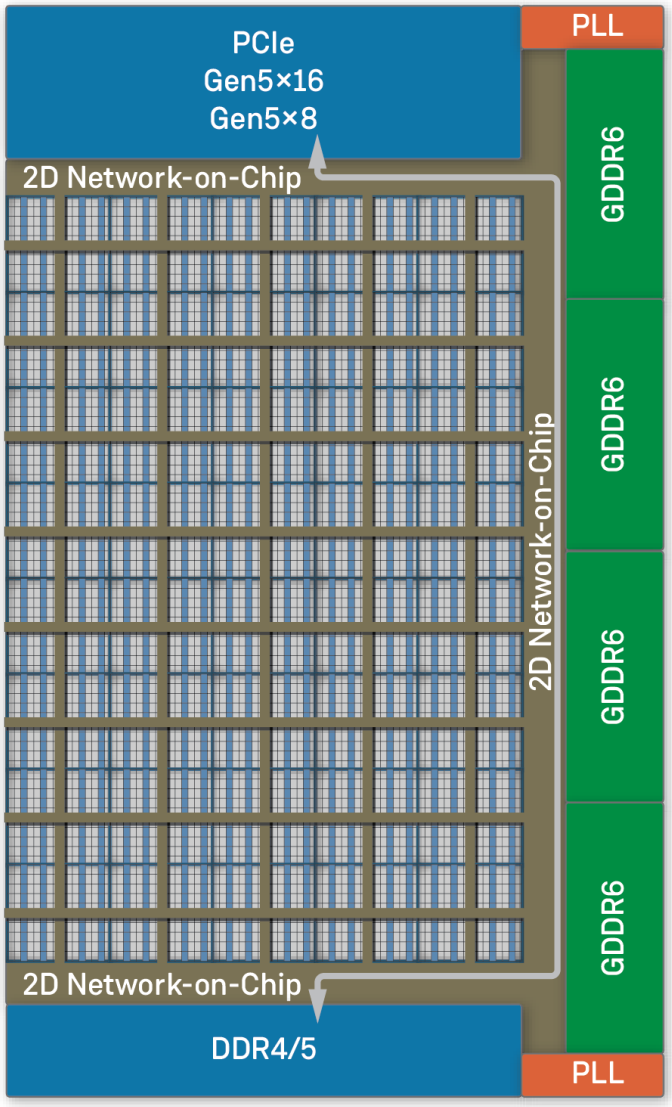

Figure 13 • Data Flow from PCIe Interface to DDR4 Through the NoC as seen on AC7t1400/AC7t1500

NoC Addressing for DDR4

The table below shows how DDR4 NoC addressing is established.

Table 6 • DDR4 NoC Addressing Scheme

Address Bit	41	40	39	38	37	36	35	34	33	32	31	30	29	28	..	0
DDR4	0	1	Memory Address													

The target ID for DDR4 is represented by two most significant bits, and the remaining bits, Addr[39:0], represent the DDR4 external memory address.

The address depends on the device density. For example for a 128-Gb device (16 GB) requires a 34-bit address, Addr[33:0], on the AXI ports because AXI uses a byte addressing scheme. The remaining bits, Addr[39:34], should be set to zero.

NoC Addressing for DDR5

The table below shows how DDR5 NoC addressing is established. On AC7t800, the DDR IP has two ports that can both write to the available DDR memory. It is also possible to interleave access between the two ports.

Table 7 • DDR5 NoC Addressing Scheme

Address Bit	41	40	39	38	37	36	35	34	33	32	31	30	29	28	..	0
DDR5	0	1	Port	Memory Address												
DDR5 interleaved access	1	0	0	Address												

Table Note

Port can be 0 or 1

The target ID for DDR5 is represented by thee most significant bits, and the remaining bits, Addr[38:0], represent the DDR4 external memory address.

Connectivity to the Direct Connect Interface (Only Applicable to AC7t1400/AC7t1500)

The DDR4 subsystem also enables a connection directly to the fabric through the direct connect interface, a 512-bit AXI slave interface which connects the DDR memory controller to master logic in the FPGA. This AXI interface:

- Exposes the clocks and resets which are outputs from the DDR subsystem and are connected to the fabric cluster
- Runs at 400 MHz, supporting a DDR data rate of 3.2 Gbps

Direct Connect Interface Addressing for DDR4

The address bus width for DCI is set to 40 bits and is represented exactly the same way as for the NoC Addr[39:0] bits.

Bypass Interface

The DDR4/5 PHY has the provision of being bypassed, allowing the FPGA core to control its input and output pins directly as GPIO. PHY bypass is achievable by turning on the bypass mode enable control bits. There are a total of 158 DDR4 pins that can utilized as GPIO in addition to 64 GPIO on the 7t1500/7t1400 device. There are a total of 170 DDR4/5 pins that can be utilized as GPIO in addition to 76 GPIO on the AC7t800 device.

Table 8 • Support Specifications for SPIO

Feature	AC7t1500 SPIO	AC7t800 SPIO
Availability	Only available when the DDR4 interface is not exercised, and the DDR4 PHY is set in bypass mode.	Only available when the DDR4/5 interface is not exercised, and the DDR4/5 PHY is set in bypass mode.
Max frequency	These I/O are meant to drive low-frequency interfaces for test/debug purposes such as boundary scan, DC I/O parametric testing, SoC-level ATPG I/O, DDR4 memory connectivity testing, etc., running at a maximum of 100 Mhz(†)	These I/O are meant to drive low-frequency interfaces for test/debug purposes such as boundary scan, DC I/O parametric testing, SoC-level ATPG I/O, DDR4/5 memory connectivity testing, etc., running at a maximum of 100 Mhz.(†)
Supported I/O standards	Not compliant with any official I/O standard. These I/O work at 1.2V ±5% (with provision of certain on-die termination schemes)	Not compliant with any official I/O standard. These I/O work at 1.2V ±5% (with provision of certain on-die termination schemes)
Signal direction	The direction of these pins is retained from that of the DDR4 interface.	The direction of these pins is retained from that of the DDR4/5 interface.
Total count	158	170

Table Note

† It is difficult to determine the maximum rate since these are not clock paths but rather combinatorial paths. The maximum frequency depend on user logic in the fabric, board-level skews and delays. In general, these I/O can operate up to 100 MHz.

Chapter 7 : DDR Core and Interface Signals

The Speedster AC7t1400/AC7t1500 FPGA has a single DDR4 hard IP core that can be enabled and configured by the user in ACE. The DDR4 subsystem for direct connect (DC) interface connection comprises:

- Clock and Reset Signals (page 31)
- Error and Interrupt Signals (page 31)
- DDR4 Subsystem-to-Core AXI4 Interface Signals (page 33)
- DDR4 Subsystem to Memory Interface Signals on AC7t1400/AC7t1500 (page 37)

This section below lists all the signals that a user requires to bring up in a design that interfaces with the DDR4 subsystem on the Speedster7t FPGA.

> **Note**
>
> The DDR4 ports have a logical and consistent naming scheme within ACE, consisting of a `<prefix>_function`. The `<prefix>` is user defined.

Clock and Reset Signals

The following table summarizes the clock and reset signals from DDR4 subsystem that tie into the fabric. When using DCI, these pins should be tied to the clock and reset pins of the DCI AXI module. This is only applicable on AC7t1400/AC7t1500.

Table 9 • DDR4 Subsystem Clock and Reset Signals

Pin Name	Direction	Width	Description
`<prefix>_clk`	Input	1	Clock from DDR4 subsystem to the FPGA core at 400 Mhz max rate
`<prefix>_rstn`	Input	1	Reset from DDR4 subsystem to the FPGA core

Error and Interrupt Signals

The following table lists the error and interrupt signals in the DDR4 subsystem.

Table 10 • DDR4 Subsystem Error and Interrupt Signals

Pin Name	Direction	Width	Description
<prefix>_ecc_corrected_err_irq	Output	1	ECC corrected error interrupt. This interrupt is asserted when a correctable ECC error is detected at the DFI
<prefix>_ecc_corrected_err_irq_fault	Output	1	ECC corrected error fault. This signal is a version of ecc_corrected_err_intr.(†)
<prefix>_ecc_uncorrected_err_irq	Output	1	ECC uncorrected error interrupt. This interrupt is asserted when a uncorrectable ECC error is detected
<prefix>_ecc_uncorrected_err_irq_fault	Output	1	ECC uncorrected error fault. This signal is a version of ecc_uncorrected_err_intr.(†)
<prefix>_dfi_alert_err_irq	Output	1	DFI alert interrupt from the DDR4 PHY
<prefix>_par_waddr_err_irq	Output	1	AXI write address parity error interrupt
<prefix>_par_waddr_err_irq_fault	Output	1	AXI write address parity error fault. This signal is a version of par_waddr_err_intr.(†)
<prefix>_par_raddr_err_irq	Output	1	AXI read address parity error interrupt
<prefix>_par_raddr_err_irq_fault	Output	1	AXI read address parity error fault. This signal is a version of par_raddr_err_intr.(†)
<prefix>_par_wdata_err_irq	Output	1	On-chip write data parity error interrupt
<prefix>_par_wdata_err_irq_fault	Output	1	On-chip write data parity error fault. This signal is a version of par_wdata_err_intr.(†)
<prefix>_par_rdata_err_irq	Output	1	On-chip read data parity error interrupt
<prefix>_par_rdata_err_irq_fault	Output	1	On-chip read data parity error fault. This signal is a version of par_rdata_err_intr.(†)
<prefix>_phy_irq_n	Output	1	Interrupt from PHY indicating alert conditions. User must treat this signal as asynchronous signal and must use a simple 2-d synchronizer.

Pin Name	Direction	Width	Description

Table Note

† This signal cannot be disabled or forced through register.

DDR4 Subsystem-to-Core Direct Connect Interface Signals

The table below shows the controller to core DC interface signals

Table 11 • DDR4 Subsystem Controller-to-Fabric Interface Signals

Pin Name	Direction	Width	Description
<prefix> _dc_awid	Output	8	AXI write address ID. Identification tag for the write address group of signals.
<prefix> _dc_awaddr	Output	40	AXI write address. The address of the first transfer in a write burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in a burst.
<prefix> _dc_awlen	Output	8	AXI write burst Length. The number of transfers in a burst associated with the write address.
<prefix> _dc_awsize	Output	3	AXI write burst size. The size of each transfer in a burst. Byte lane strobes indicate exactly which byte lanes to update.
<prefix> _dc_awburst	Output	2	AXI write burst type. Coupled with the size, burst type details how the address for each transfer within a burst is calculated.
<prefix> _dc_awlock	Output	1	AXI write lock type. Provides additional information about the atomic characteristics of the transfer.
<prefix> _dc_awcache	Output	4	AXI write cache type. Indicates the buffer-able, cache-able, write-through, write-back, and allocate attributes of the transaction.(1).

Pin Name	Direction	Width	Description
<prefix> _dc_awprot	Output	3	AXI write protection Type. Indicates the normal, privileged, or secure protection level of the transaction and whether the transaction is a data access or an instruction access.(1)
<prefix> _dc_awqos	Output	4	AXI write quality of service. Sideband signal to indicate the quality-of-service attributes of the write transaction. The awqos signalling is sticky, that is, it must remain stable when awvalid is asserted and awready is de-asserted. This signal determines the transaction priority for port arbitration. Higher values signify higher priority.
<prefix> _dc_awregion	Output	4	AXI4 write address region signal.(1).
<prefix> _dc_awex_auto_precharge	Output	1	AXI auto-precharge signal for write command. This port is for write address channel signal. This signal is valid when awvalid is high.
<prefix> _dc_awex_parity	Output	1	AXI write address parity. Parity is calculated for the whole address. Type of parity should match the configuration in memory controller register for parity
<prefix> _dc_awex_poison	Output	1	AXI write poison. Sideband signal to indicate an invalid write transaction. When asserted, no data is written to the memory. If not needed, the signal must be tied to low.
<prefix> _dc_awex_urgent	Output	1	AXI write urgent. Sideband signal to indicate a write urgent transaction. When asserted, if wr_port_urgent_en register is set, causes the port arbiter to switch immediately to write. It can be asserted anytime and is not associated to any particular command.
<prefix> _dc_awvalid	Output	1	AXI write address valid. Indicates that the valid write address and control information are available.
<prefix> _dc_awready	Input	1	AXI write address ready. Indicates that the slave is ready to accept an address and associated control signals.
<prefix> _dc_wdata	Output	512	AXI write data.

Pin Name	Direction	Width	Description
<prefix> _dc_wstrb	Output	64	AXI write data byte strobe. Indicates which byte lanes to update in memory.
<prefix> _dc_wlast	Output	1	AXI write last. Indicates the last transfer in a write burst.
<prefix> _dc_wex_parity	Output	64	AXI write data parity.
<prefix> _dc_wvalid	Output	1	AXI write valid. Indicates that valid write data and strobes are available.
<prefix> _dc_wready	Input	1	AXI write ready. Indicates that the slave can accept the write data.
<prefix> _dc_bid	Input	8	AXI write response ID. Must match the awid value of the write transaction to which the slave is responding
<prefix> _dc_bresp	Input	2	AXI write response. Indicates the status of the write transaction
<prefix> _dc_bvalid	Input	1	AXI write response Valid. Indicates that a valid write response is available
<prefix> _dc_bready	Output	1	AXI write response Ready. Indicates that the master can accept the write response information.
<prefix> _dc_arid	Output	8	AXI read address ID. Identification tag for the read address group of signals.
<prefix> _dc_araddr	Output	40	AXI read address. The address of the first transfer in a read burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in a burst.
<prefix> _dc_arlen	Output	8	AXI read burst length. The number of transfers in a burst associated with the read address.
<prefix> _dc_arsize	Output	3	AXI read burst size. The size of each transfer in a burst.
<prefix> _dc_arburst	Output	2	AXI read burst type. Coupled with the size, burst type details how the address for each transfer within a burst is calculated.

Pin Name	Direction	Width	Description
<prefix> _dc_arlock	Output	1	AXI read lock type. Provides additional information about the atomic characteristics of the transfer.
<prefix> _dc_arcache	Output	4	AXI read cache type. Provides additional information about the cacheable characteristics of the transfer.(1).
<prefix> _dc_arprot	Output	3	AXI read protection Type. Provides protection unit information for the transaction.(1)
<prefix> _dc_arqos	Output	4	AXI read quality of service. Sideband signal to indicate the quality of service attributes of the read transaction. The arqos signalling is sticky, that is, it must remain stable when arvalid is asserted and arready is de-asserted. This signal determines the transaction priority for port arbitration. Higher values signify higher priority. This signal determines also the priority of the read transfer going into the CAM depending on the programming of the PCFGQOS0_n register in memory controller
<prefix> _dc_arregion	Output	4	AXI 4 read address region signal.(1)
<prefix> _dc_arex_auto_precharge	Output	1	AXI auto-precharge signal for read command. This port is for read address channel signal. This signal is valid when arvalid is high.
<prefix> _dc_arex_parity	Output	1	AXI read address parity. Parity is calculated for the whole address. Type of parity should match the configuration in memory controller register for parity.
<prefix> _dc_arex_poison	Output	1	AXI read poison. Sideband signal to indicate an invalid read transaction. When asserted, all zeros are returned at the output. If not needed, signal must be tied to zero.
<prefix> _dc_arex_urgent	Output	1	AXI read Urgent. Off-band signal to indicate a read urgent transaction. When asserted, if rd_port_urgent_en register is set, causes the port arbiter to switch immediately to read. It can be asserted anytime, it is not associated to any particular command.
<prefix> _dc_arvalid	Output	1	AXI read address Valid. Indicates that valid read address and control information are available.

Pin Name	Direction	Width	Description
<prefix>_dc_arready	Input	1	AXI read address Ready. Indicates that the slave is ready to accept an address and associated control signals
<prefix> _dc_rid	Input	8	AXI read ID. Must match the arid value of the read transaction to which the slave is responding
<prefix> _dc_rdata	Input	512	AXI read Data.
<prefix> _dc_rresp	Input	2	AXI read Response. Indicates the status of the read transfer.
<prefix> _dc_rlast	Input	1	AXI read Last. Indicates the last transfer in a read burst.
<prefix>_dc_rex_parity	Input	64	AXI read parity/ECC. Generated by the memory controller. Byte wise parity is generated based on parity type selection in configuration of memory controller register for parity.
<prefix> _dc_rvalid	Input	1	AXI read Valid. Indicates that the required read data is available and the read transfer can complete.
<prefix> _dc_rready	Output	1	AXI read Ready. Indicates that the master can accept the read data and response information.

Table Note

1. This signal is not used by the controller and must be tied off to 0.

DDR4 Subsystem to Memory Interface Signals on AC7t1400/ AC7t1500

The table below summarizes the DDR4 external memory to PHY interface signals:

Table 12 • DDR4 Subsystem to Memory Interface Signals

Pin Name	Direction	Width	Description
<prefix>**_bp_memreset_l**	Output	1	SDRAM reset pin controlled by PHY.

Pin Name	Direction	Width	Description
<prefix>_a[13:0]	Output	14	SDRAM address bus.
<prefix>_a17	Output	1	SDRAM address signal.
<prefix>_act_n	Output	1	SDRAM activate input command.
<prefix>_ba[1:0]	Output	2	SDRAM bank address select within a bank group.
<prefix>_bg[1:0]	Output	2	SDRAM bank group select.
<prefix>_alert_n	input	1	SDRAM alert signal.
<prefix>_cas_n	Output	1	SDRAM CAS control signal.
<prefix>_cid	Output	1	SDRAM chip Id select; These inputs are used only when devices are stacked for x4 and x8 configurations using TSV.
<prefix>_ck_n[3:0]	Output	4	SDRAM differential clock signal.
<prefix>_ck_p[3:0]	Output	4	SDRAM differential clock signal.
<prefix>_cke[3:0]	Output	4	SDRAM clock enable control signal
<prefix>_cs_n[3:0]	Output	4	SDRAM chip select.
<prefix>_dq_0[7:0]	Bidir.	8	SDRAM bidirectional data bus, byte lane 0.
<prefix>_dq_1[7:0]	Bidir.	8	SDRAM bidirectional data bus, byte lane 1.
<prefix>_dq_2[7:0]	Bidir.	8	SDRAM bidirectional data bus, byte lane 2.
<prefix>_dq_3[7:0]	Bidir.	8	SDRAM bidirectional data bus, byte lane 3.
<prefix>_dq_4[7:0]	Bidir.	8	SDRAM bidirectional data bus, byte lane 4.
<prefix>_dq_5[7:0]	Bidir.	8	SDRAM bidirectional data bus, byte lane 5.
<prefix>_dq_6[7:0]	Bidir.	8	SDRAM bidirectional data bus, byte lane 6.
<prefix>_dq_7[7:0]	Bidir.	8	SDRAM bidirectional data bus, byte lane 7.
<prefix>_dq_8[7:0]	Bidir.	8	SDRAM bidirectional data bus, byte lane 8.
<prefix>_udqs_n[8:0]	Bidir.	9	SDRAM differential strobes, used for ×4 mode.

Pin Name	Direction	Width	Description
<prefix>_udqs_p[8:0]	Bidir.	9	SDRAM differential strobes, used for ×4 mode.
<prefix>_ldqs_n[8:0]	Bidir.	9	SDRAM differential strobes, used for ×8 mode.
<prefix>_ldqs_p[8:0]	Bidir.	9	SDRAM differential strobes, used for ×8 mode.
<prefix>_odt[3:0]	Output	4	SDRAM on-die termination control signal.
<prefix>_par	Output	1	SDRAM parity bit for command and address.
<prefix>_ras_n	Output	1	SDRAM RAS control signal.
<prefix>_we_n	Output	1	SDRAM write enable control signal.
<prefix>**_dm_dbi_udqs_p[8:0]**	Bidir.	9	SDRAM data mask/data bus inversion signal.

More information on the DDR device-level pins can be found in the Speedster7t Pin Connectivity User Guide[13] (UG084)[14], and the power-level requirements for the DDR signals can be found in the Speedster7t Power User Guide[15] (UG087)[16].

DDR4/5 Subsystem to Memory Interface Signals on AC7t800

The Speedster7t800 FPGA has a single DDR4/5 hard IP core that can be enabled and configured by the user in ACE. This device does not support DCI. Therefore, none of these pins are accessible via the FPGA fabric.

The table below summarizes the DDR5 external memory to PHY interface signals:

Table 13 • DDR5 Subsystem to Memory Interface Signals

Pin Name	Direction	Width	Description
<prefix>**_bp_memreset_l**	Output	1	SDRAM reset pin controlled by PHY.
<prefix> *_a0_*ca_b1	Output	1	Command/Address (CA) signals Channel B
<prefix> *_par_a*	Output	1	Command/Address (CA) signals Channel B (CA_B0 on RDIMM and CA_B13 on UDIMM/ component)

13 https://www.achronix.com/documentation/speedster7t-pin-connectivity-user-guide-ug084
14 https://www.achronix.com/documentation/speedster7t-pin-connectivity-user-guide-ug084
15 https://www.achronix.com/documentation/speedster7t-power-user-guide-ug087
16 https://www.achronix.com/documentation/speedster7t-power-user-guide-ug087

Pin Name	Direction	Width	Description
<prefix>_a2_null	Output	1	Command/Address (CA) signals Channel A
<prefix>_a3_ca_a5	Output	1	Command/Address (CA) signals Channel A (CA_A5 on RDIMM and CA_A10 on UDIMM/component)
<prefix>_a4_null	Output	1	Command/Address (CA) signals
<prefix>_a5_ca_a6	Output	1	Command/Address (CA) signals Channel A (CA_A6 on RDIMM and CA_A9 on UDIMM/ component)
<prefix>_a6_null	Output	1	Command/Address (CA) signals Channel A
<prefix>_a7_null	Output	1	Command/Address (CA) signals Channel A
<prefix>_a8_ca_a4	Output	1	Command/Address (CA) signals Channel A (CA_A4 on RDIMM and CA_A7 on UDIMM/component)
<prefix>_a9_ca_a1	Output	1	Command/Address (CA) signals Channel A (CA_A1 on RDIMM and CA_A3 on UDIMM/component)
<prefix>_a10_null	Output	1	Command/Address (CA) signals Channel B
<prefix>_a11_ca_a3	Output	1	Command/Address (CA) signals Channel A (CA_A3 on RDIMM and CA_A5 on UDIMM/component)
<prefix>_a12_null	Output	1	Command/Address (CA) signals Channel A
<prefix>_a13_null	Output	1	Command/Address (CA) signals Channel B
<prefix>_a17_rspn_a1	Output	1	Command/Address (CA) signals (RSPN_A1 on RDIMM and CA_B3 on UDIMM/component)
<prefix>_act_n_null	Output	1	Command/Address (CA) signals Channel A
<prefix>_ba0_ca_b2	Output	1	Command/Address (CA) signals (CA_B2 on RDIMM and CA_B11 on UDIMM/component)
<prefix>_ba1_null	Output	1	Command/Address (CA) signals Channel A
<prefix>_bg0_ca_a0	Output	1	Command/Address (CA) signals Channel A
<prefix>_bg1_ca_a2	Output	1	Command/Address (CA) signals Channel A (CA_A2 on RDIMM and CA_A1 on UDIMM/component)

Pin Name	Direction	Width	Description
<prefix>_c0_ca_b4	Output	1	Command/Address (CA) signals Channel B (CA_B4 on RDIMM and CA_B6 on UDIMM/component)
<prefix>_c1_rspn_a0	Output	1	Command/Address (CA) signals Channel B (RSPN_A0 on RDIMM and CA_B5 on UDIMM/component)
<prefix>_c2_ca_b6	Output	1	Command/Address (CA) signals Channel B (CA_B6 on RDIMM and CA_B4 on UDIMM/component)
<prefix>_cas_n_null	Output	1	Command/Address (CA) signals Channel B
<prefix>_cke0_csa0	Output	1	Chip Select Channel A
<prefix>_cke1_csa1	Output	1	Chip Select Channel A
<prefix>_cke2_csa2	Output	1	Chip Select Channel A
<prefix>_clk0_c_ck_a0_c	Output	1	Differential clock
<prefix>_clk0_t_ck_a0_t	Output	1	Differential clock
<prefix>_clk1_c_null	Output	1	Differential clock
<prefix>_clk1_t_null	Output	1	Differential clock
<prefix>_clk2_c_ck_b0_c	Output	1	Differential clock
<prefix>_clk2_t_ck_b0_t	Output	1	Differential clock
<prefix>_clk3_c_null	Output	1	Differential clock
<prefix>_clk3_t_null	Output	1	Differential clock
<prefix>_cs_n0_ca_b5	Output	1	Command/Address (CA) signals Channel B (CA_B5 on RDIMM and CA_B2 on UDIMM/component)
<prefix>_cs_n1_rspn_b0	Output	1	Command/Address (CA) signals Channel B (RSPN_B1 on RDIMM and CA_B0 on UDIMM/component)

Pin Name	Direction	Width	Description
<prefix>_cs_n3_rspn_b1	Output	1	Command/Address (CA) signals Channel B
<prefix>_dm_dbi_udqs_t[9:0]	Bidir.	10	SDRAM differential strobes, used for ×4/x16 mode.
<prefix>_dq_0[7:0]	Bidir.	8	SDRAM bidirectional data bus, byte lane 0 (data for bus for channel 0).
<prefix>_dq_1[7:0]	Bidir.	8	SDRAM bidirectional data bus, byte lane 1 (data for bus for channel 0).
<prefix>_dq_2[7:0]	Bidir.	8	SDRAM bidirectional data bus, byte lane 2 (data for bus for channel 0).
<prefix>_dq_3[7:0]	Bidir.	8	SDRAM bidirectional data bus, byte lane 3 (data for bus for channel 0).
<prefix>_dq_4[7:0]	Bidir.	8	SDRAM bidirectional data bus, byte lane 4 (data for bus for channel 1).
<prefix>_dq_5[7:0]	Bidir.	8	SDRAM bidirectional data bus, byte lane 5 (data for bus for channel 1).
<prefix>_dq_6[7:0]	Bidir.	8	SDRAM bidirectional data bus, byte lane 6 (data for bus for channel 1).
<prefix>_dq_7[7:0]	Bidir.	8	SDRAM bidirectional data bus, byte lane 7 (data for bus for channel 1).
<prefix>_dq_8[7:0]	Bidir.	8	SDRAM bidirectional data bus, byte lane 8 (ECC data for channel 0).
<prefix>_dq_9[7:0]	Bidir.	8	SDRAM bidirectional data bus, byte lane 9(ECC data for channel 0).
<prefix>_ldqs_c[9:0]	Bidir.	10	SDRAM differential strobes, used for ×8 mode.
<prefix>_ldqs_t[9:0]	Bidir.	10	SDRAM differential strobes, used for ×8 mode.
<prefix>_malert_n_malert_n	Output	1	MALERT
<prefix>_odt0_csb0	Output	1	Chip Select Channel B
<prefix>_odt1_csb1	Output	1	Chip Select Channel B

Pin Name	Direction	Width	Description
<prefix>_odt2_csb2	Output	1	Chip Select Channel B
<prefix>_odt3_csb3	Output	1	Chip Select Channel B
<prefix>_par_ca_b0	Output	1	Command/Address (CA) signals Channel A (PAR_A on RDIMM and CA_A12 on UDIMM/ component)
<prefix>_ras_n_null	Output	1	Command/Address (CA) signals Channel B
<prefix>_udqs_c[9:0]	Bidir.	10	SDRAM differential strobes, used for ×4/x16 mode.
<prefix>_we_n_ca_b3	Bidir.	1	Command/Address (CA) signals (CA_B3 on RDIMM and CA_B8 on UDIMM/component)

More information on the DDR device-level pins can be found in the Speedster7t Pin Connectivity User Guide[17] (UG084)[18], and the power-level requirements for the DDR signals can be found in the Speedster7t Power User Guide[19] (UG087)[20].

17 https://www.achronix.com/documentation/speedster7t-pin-connectivity-user-guide-ug084
18 https://www.achronix.com/documentation/speedster7t-pin-connectivity-user-guide-ug084
19 https://www.achronix.com/documentation/speedster7t-power-user-guide-ug087
20 https://www.achronix.com/documentation/speedster7t-power-user-guide-ug087

Chapter 8 : DDR IP Software Representation in ACE

Overview

The DDR Interface IP Generation in ACE is a GUI that helps generate and integrate the DDR subsystem in a Speedster7t FPGA based on specific inputs provided by the user. The Speedster7t I/O Ring Toolkit in ACE supports the integration of the chosen IP for the user design and allows the user to select the pin placements and visualize package routing. Once the desired configuration is achieved via the IO Ring Toolkit, the ACE tool generates a bitstream for the IP interface which is independent of the bitstream generated from the FPGA fabric. The tool further integrates both these bitstreams into a single full-chip bitstream that enables configuration of a Speedster7t device.

The following steps provide a brief description on creating a DDR IP interface user design:

Step 1 – Create a Project

Create a project in ACE, and then in the 'Project perspective', select the target device. Selecting the device ensures that the appropriate IP options are available in the IP Perspective window in ACE

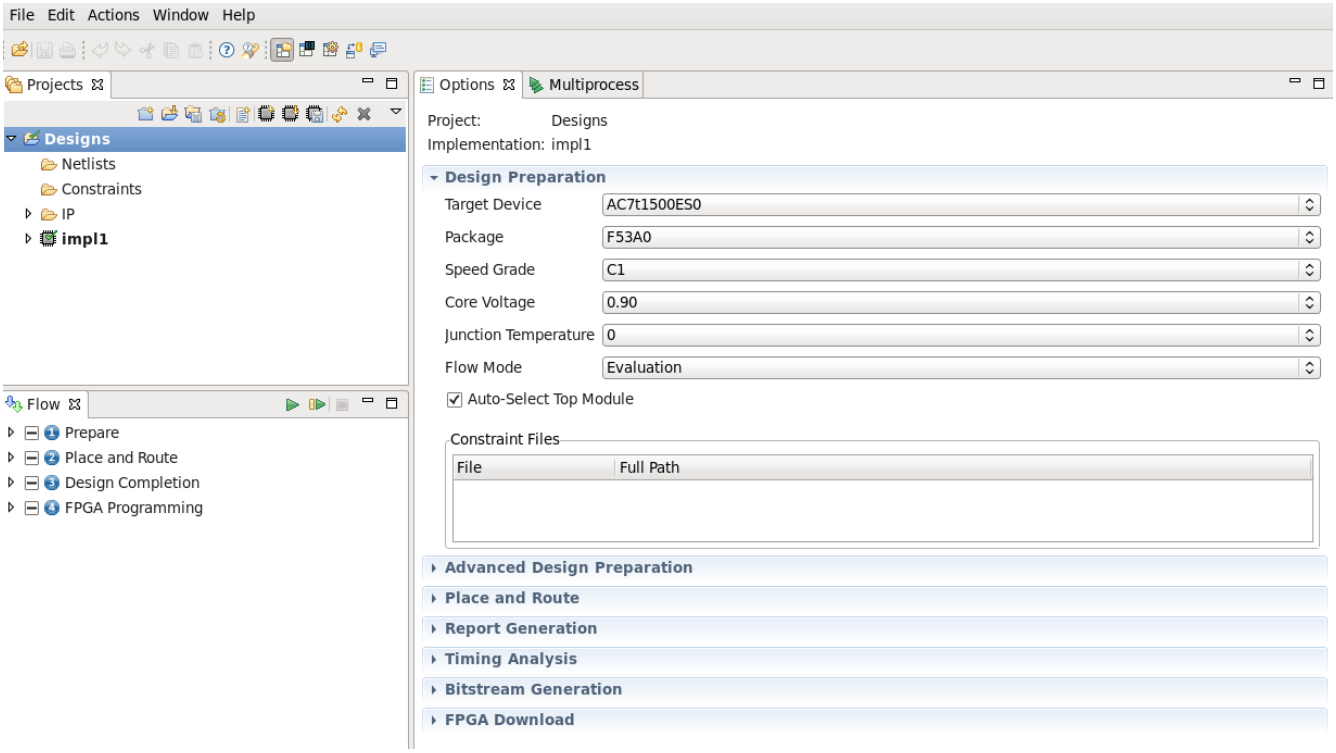

Figure 14 • Design Preparation Options in the ACE Project

Step 2 – Configure the Programmable I/O

Switch to the 'IP Configuration' perspective and select the **Programmable I/O IP** from the Speedster7t **IO Ring** to create the external input clock source; select **Add** new I/O and provide the instance name, bank type, signal type, I/O standard, the desired ball placement and frequency for the I/O. Once the selection is made, the Layout Diagram highlights the chosen I/O. The figure below shows a CLKIO being created. The programmable I/O ACXIP file will also be used for any other top-level GPIO or CLKIO, and multiple I/O can be added in the same ACXIP file.

> **Note**
>
> The external reset inputs also have to be configured in similar fashion. This capability will be available in future ACE releases.

The 'IP Problems' window highlights any errors or warnings that occurred while configuring the programmable I/O. Since the DDR4 interface is on the south edge of the FPGA, the south-west or south-east PLL clocks are preferable.

> **Note**
>
> Actual signal names are prefixed with whatever was provided at IP configuration.

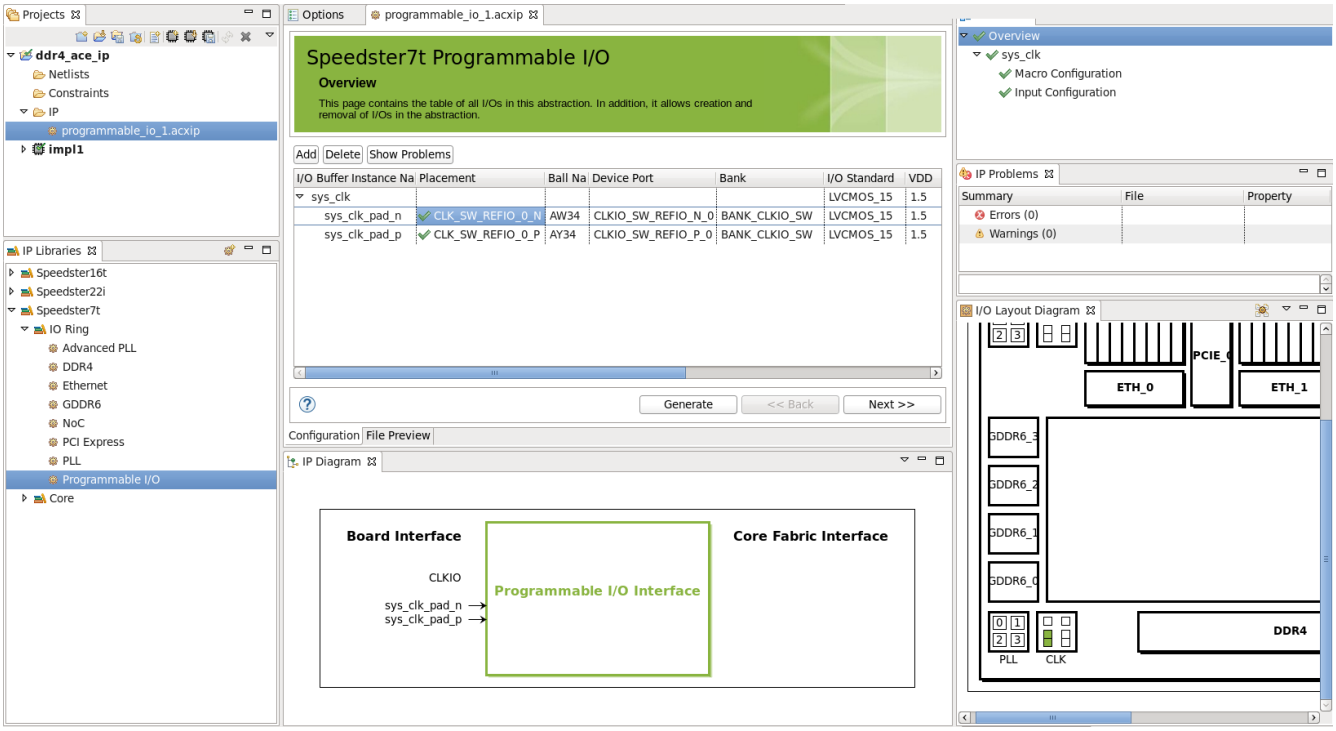

Figure 15 • Programmable I/O IP Configuration

Step 3 – Configure the PLL IP

Next, configure the PLL IP with the desired placement and appropriate clock output frequencies based on the user-specified data rate for the DDR4 interface. The DDR4 IP requires a clock running at 200 MHz to drive the NoC interface and an input reference clock at maximum of 800 MHz for the controller and PHY operations which are generated by the PLL. If the user opts for direct connect option, a third AXI clock is required to be used from the global clock signals for the direct connect AXI interface to the FPGA fabric. The number of PLL clock outputs and their respective frequencies should match the number of required clock inputs and respective rates for the subsystem to operate correctly.

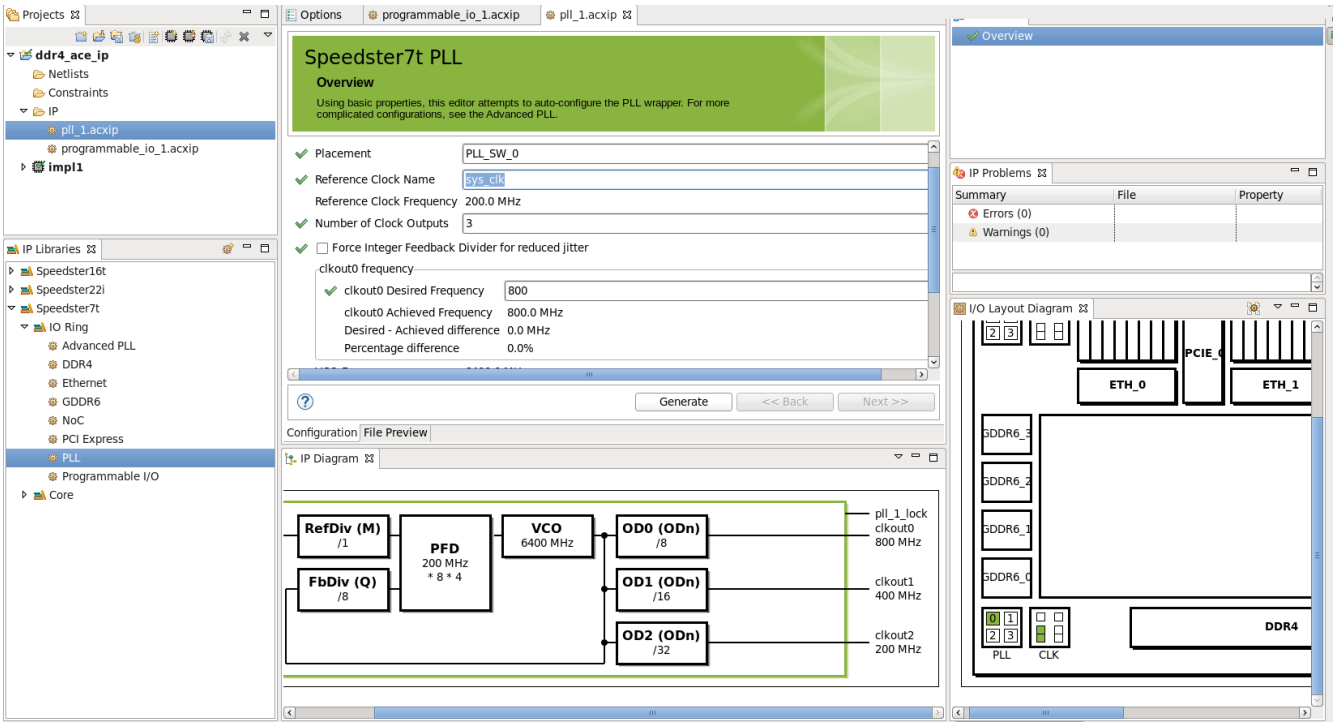

Figure 16 • PLL IP Configuration

Step 4 – Configuring the NoC

If the DDR4 subsystem interfaces with the NoC, then the user must set the NoC clock to 200 MHz. The global PLL clock output drives the NoC interface, which has been setup already in step 3; hence, the clocks with the expected range of frequency for NoC shows up at the tooltip. The NoC IP GUI also allows the user to set the NoC network access control configuration options.

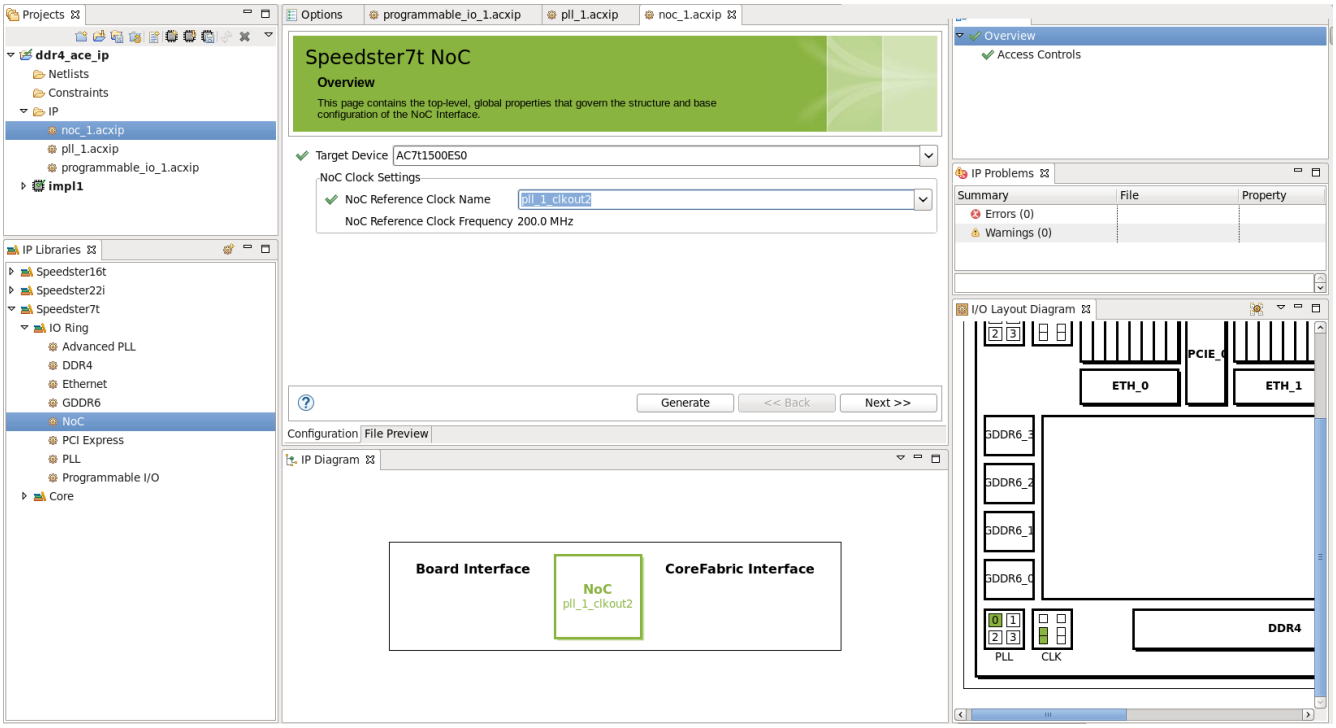

Figure 17 • NoC IP Configuration

Step 5 – Configure the DDR Interface

Next, configure the DDR subsystem interface by selecting DDR IP in the IP library section to create an ACXIP file.

If selecting a target device of AC7t1400 or AC7t1500, the "Placement" and "DDR Standard" fields must be set to "DDR4". The following tables describe the `.acxip` configuration options. If selecting a target device of AC7t800, the "Placement" must be set to "DDR5" and the "DDR Standard" field can be set to either "DDR5" or "DDR4".

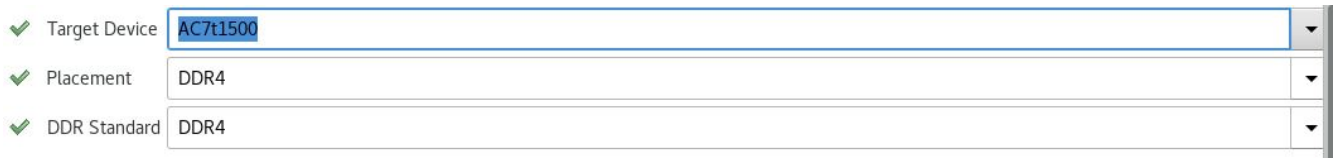

Figure 18 • Example DDR4 Placement Settings on AC7t1500

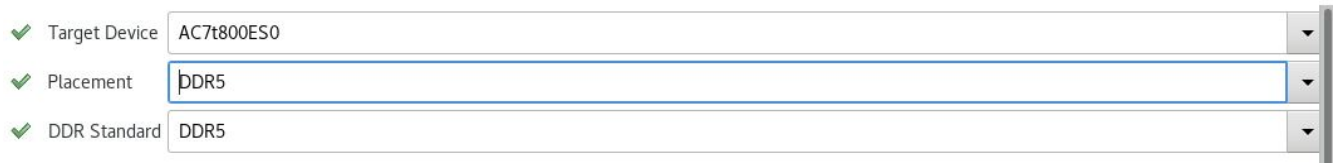

Figure 19 • Example DDR5 Placement Settings on AC7t800ES0

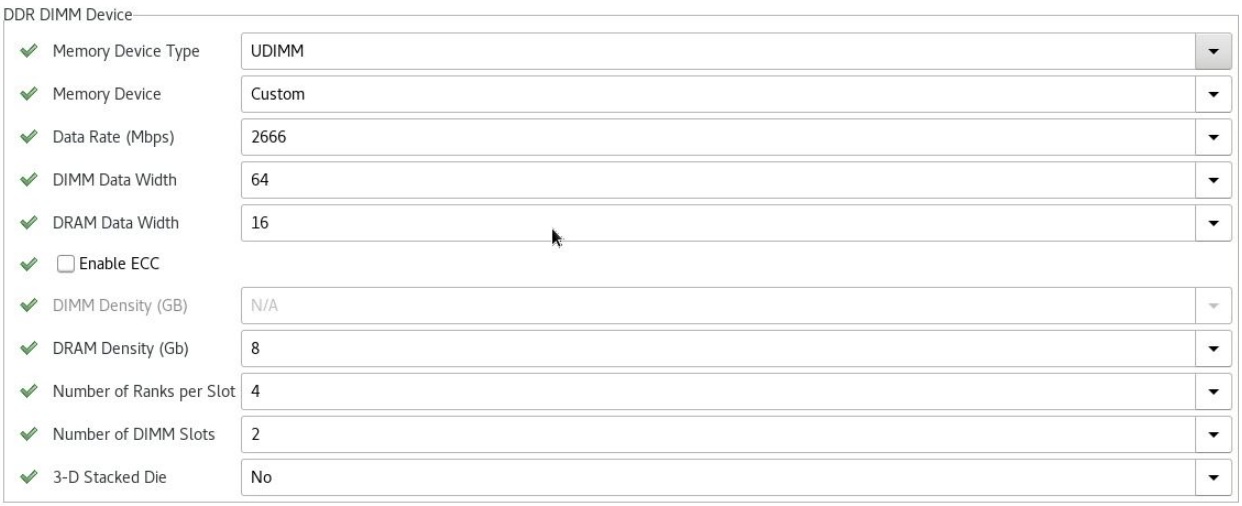

Figure 20 • DDR DIMM Device settings

Table 14 • DDR DIMM Device settings

Option	Description
Memory Device Type	Device type for selected memory interface: • Available options for DDR4 are UDIMM, RDIMM, LRDIMM, SODIMM, and Component. • Available options for DDR5 are UDIMM, RDIMM, and Component.
Memory Device	ACE supports a wide variety of DDR memory devices. The list of supported devices can be found in this drop-down menu. If a user cannot find their device listed, this field can be set to "Custom".
Data Rate	Supported data rates are listed in this field in Mbps. • For DDR4, the supported data rates are 3200, 2933, 2666, 2400, 2133, 1866, and 1600. • For DDR5, the supported data rates are 5600, 5200, 4800, 4400, 4000, 3600, and 3200.
DIMM Data Width	This value represents the DIMM data interface width when using a DIMM device or DQ data width when using a component.
DRAM Data Width	DRAM interface data width is selected in this field.
Enable ECC	Checking this box enables ECC. When enabled, This uses an additional data lane to store ECC data. Effective DRAM data width will be decided based on data width. One data lane will be utilized by the controller as the ECC lane.

Option	Description
DIMM Density	DIMM device density in GB.
DRAM Density	DRAM Component density in GB.
Number of Ranks per Slot	Number of chip selects used per DIMM slot, determined by DIMM device selected.
Number of DIMM Slots	Only 1 slot is supported for most devices and 2 slots are supported for dual ranked devices.
3-D Stacked Die	3DS die stacking option for selected memory, not supported.

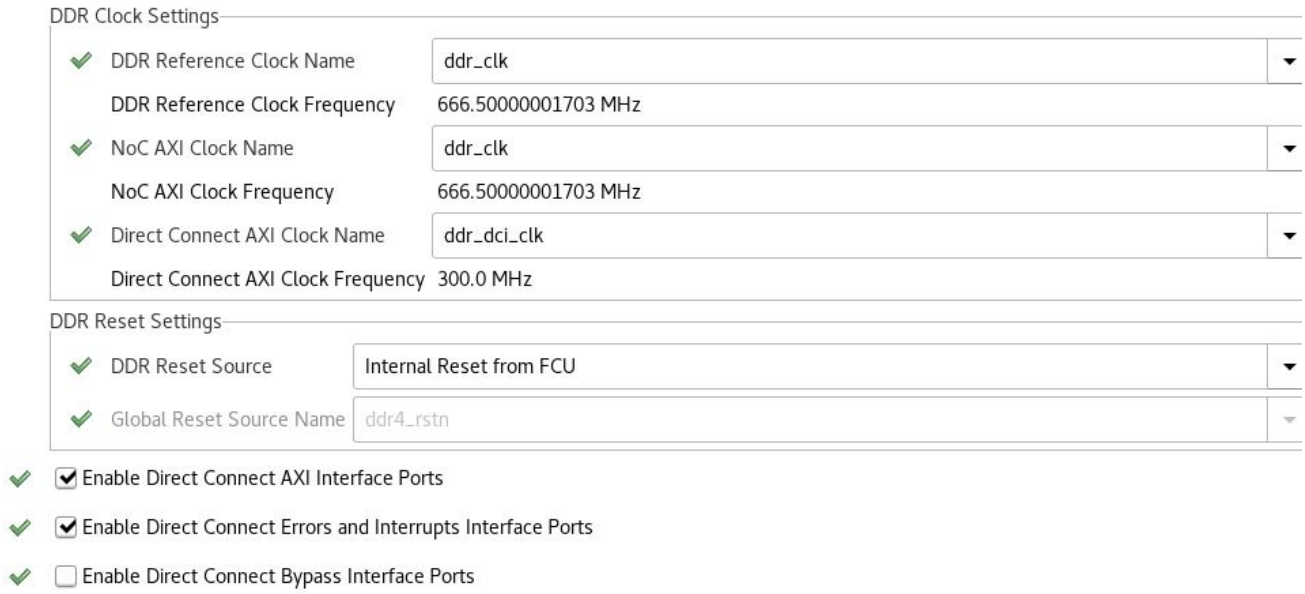

Figure 21 • DDR Clock and Reset settings

Table 15 • DDR Clock and Reset settings

Option	Description
DDR Reference Clock Name	Global clock signal name to be used for the DDR controller and PHY. Allowable range is determined by data rate.
NoC AXI Clock Name	Global clock signal name to be used for the NoC AXI port. A user can use the same clock as the DDR reference clock or a higher frequency clock to maximize NoC bandwidth. Maximum value for this clock frequency is 800 MHz.
Direct Connect AXI Clock Name	Global clock signal name for the direct connect AXI interface. This option is only applicable when using DCI to connect the fabric to the DDR controller (not applicable to AC7t800).
DDR Reset Source	DDR subsystem reset can come from the FCU (default), global reset track driven by clock I/O, or core fabric. If controlled by the FCU, reset is released when the FPGA enters user mode.

Option	Description
Global Reset Source Name	This field is only applicable if the reset is coming from the core or I/O.
Enable Direct Connect AXI Interface Ports	Enable DCI on the core fabric boundary pins (only applicable on AC7t1500/AC7t1400)
Enable Direct Connect Errors and Interrupts Interface Ports	Enable DCI errors and interrupts on the core fabric boundary pins
Enable Direct Connect Bypass Interface Ports	Enable bypass mode, which bypasses the DDR controller and PHY. In this case, the DDR I/O pins are directly connected to the core fabric.

Step 6 – Configure Achronix Device Manager

AC7t1400/AC7t1500

Configure the device manager ACXIP file. Set the target device accordingly. Ensure that the NAP is placed on the south half of the chip by setting the NAP row to 4 or less. The NAP column can be set to any column. However, for AC7t1400 devices, the Achronix device manager NAP must not be placed in the southeast corner of the fabric to avoid placement conflict with the cryptocore.

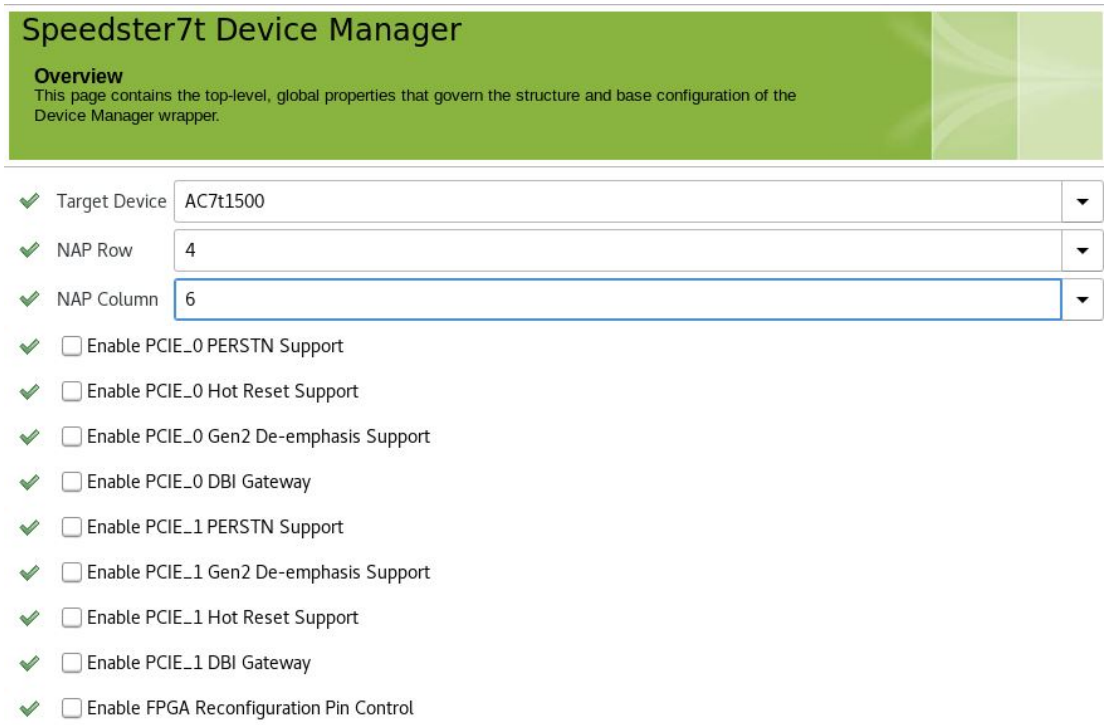

Figure 22 • Achronix Device Manager Configuration

AC7t800

Configure the Device Management System ACXIP. Set the target device accordingly and ensure that the "Enable DDR5 Training" box is checked. Also, a reference clock of 250 MHz must be applied to this subsystem.

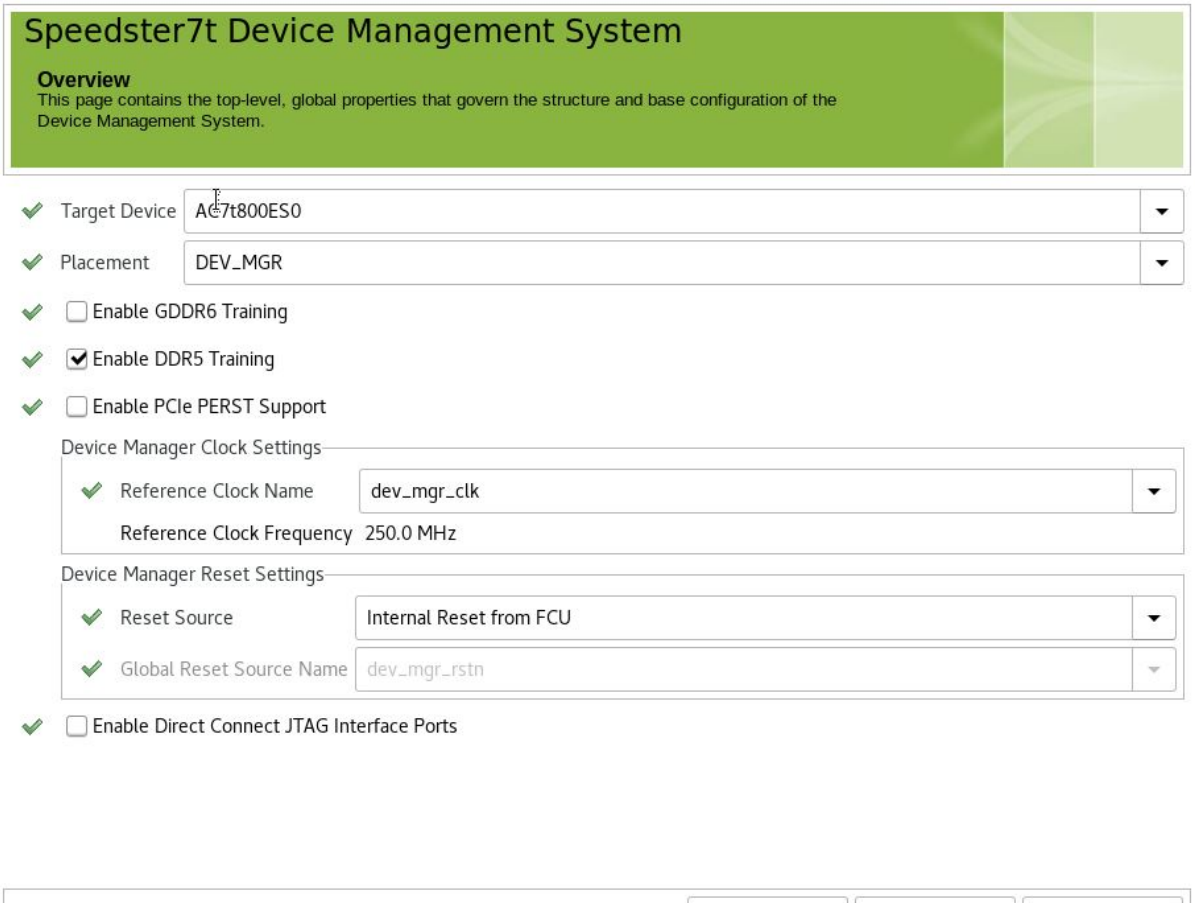

Figure 23 • Device Management System Subsystem Configuration

> **Warning!**
>
> DDR4 ADM training is not available in the bitstream flow on AC7t800 currently. This feature will be enabled in future versions of ACE.

Step 7 – Check for Errors

After all the configuration options are selected, check the 'IP Problems' window report for any errors or warnings. If there are no errors reported, the entire I/O interface with all the required IP has been integrated properly and will close timing at the specified data rate.

There is also a fully interactive 'I/O Package Diagram' view. If the user hovers over the package diagram where the DDR4 pins were placed, all information related to these pins will show up at the tooltip. The 'I/O Pin Assignments' is also an interactive map that lists all pins utilized for the DDR4 design and any other IP present in the user design.

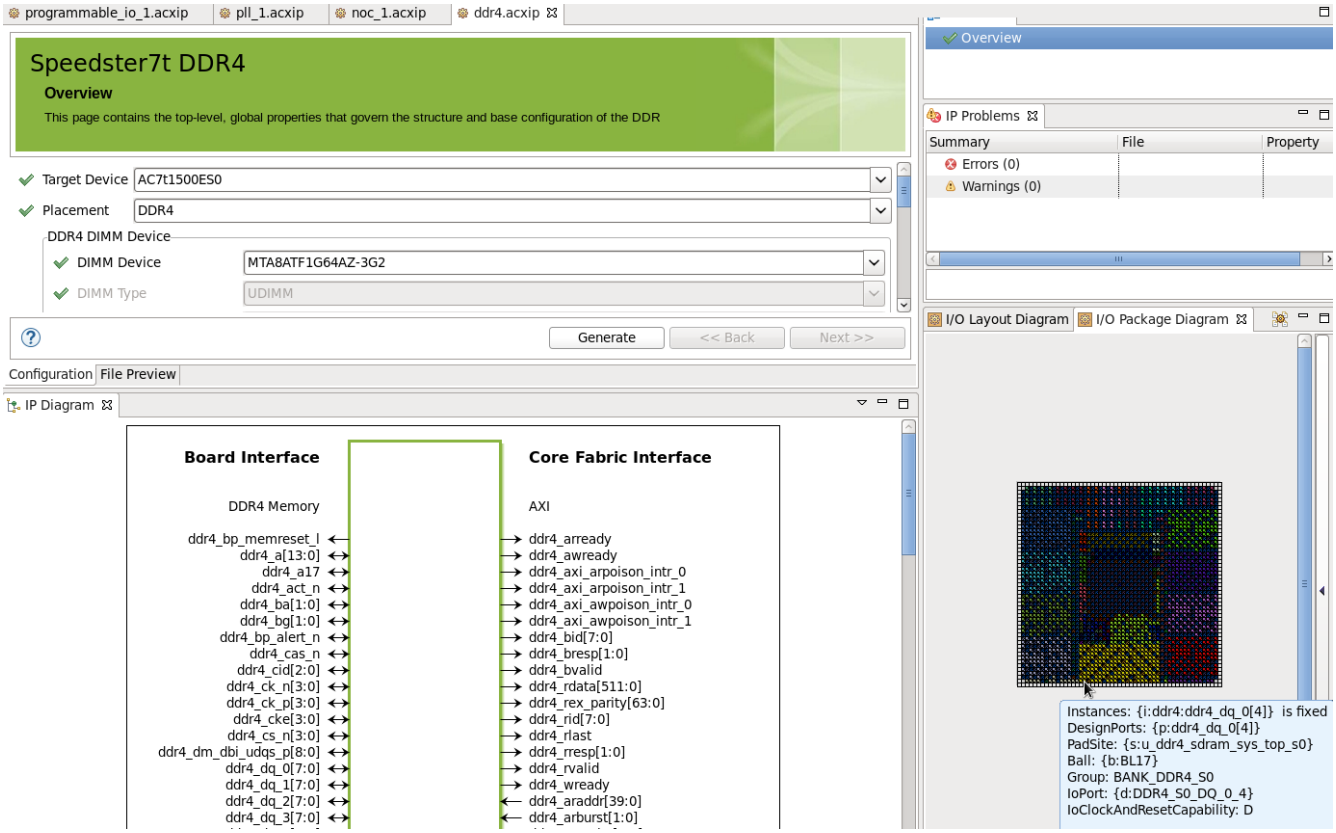

Figure 24 • DDR4 Subsystem's Interactive Tools

Step 7 – Generate the Design Files

Once the configurations are verified, click the **Generate** option in any of the ACXIP files to generate all the necessary files needed for I/O ring bitstream generation. The following files are generated:

- SDC file with timing constraints for all clocks exposed to the FPGA fabric
- PDC file with pin placements for DDR4 DC interface pins (if enabled) and all GPIO pins used (by the user design)
- Bitstream for the entire I/O ring
- The necessary simulation files to bind the fabric design with a testbench

The user can now switch to building the core design. This core design will be integrated with the bitstream generated for the I/O interface to obtain the final full-chip integrated bitstream.

Chapter 9 : Speedster7t DDR User Guide Revision History

Revision History

Version	Date	Description
1.0	19 Mar 2020	Initial release.
2.0	19 Dec 2024	▪ Added DDR support for the AC7t800. ▪ Added information on the bypass mode which allows users to enable fully independent control of the DDR4/5 I/O from user implemented logic through the fabric. ▪ Added info on Achronix device manager/device management system training since DDR training on AC7t1400/AC7t1500 and AC7t800 are no longer handled by user-implemented fabric logic. ▪ Updated software representation to reflect ACE version 10.1.