Speedster7t FPGA Datasheet (DS015)

Speedster FPGAs

Achronix
Data Acceleration

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Chapter 1 : Overview

Introducing the Speedster7t FPGA Family

The Achronix high-performance, 7nm Speedster®7t FPGA family is specifically designed to support extremely high bandwidth requirements for demanding applications including data-center workloads and networking infrastructure. The processing tasks associated with these high-performance applications, specifically those associated with artificial intelligence and machine learning (AI/ML) and high-speed networking, represent some of the most demanding processing workloads in the data center.

Several performance criteria characterize these data-center and networking workloads requiring the following abilities:

- Handle high-speed data rates from a host processor PCIe Gen5 port and up to 400 Gbps on the Ethernet ports
- Store multiple gigabytes of incoming data and to access that data quickly for processing within the FPGA
- Move massive amounts of data among the FPGA I/O ports, its internal memory, attached external memory, and its on-chip computing resources
- Process high computational workloads with tera operations per second (TOPS) performance.

The Speedster7t FPGA family that includes AC7t700, AC7t800, AC7t1400, and AC7t1500 devices can more than satisfy each of these performance criteria with appropriately scaled and optimized on-chip resources.

Handling High-Speed Incoming and Outgoing Data

For data center and networking applications, high-speed data enters an FPGA-based processing node in two fundamental ways: through PCIe connections to a host processor and via high-speed Ethernet connections. The Speedster7t FPGA family is designed to maximize data rates over these connections by implementing a number of PCIe Gen5 interfaces for the host processor connection(s) and multiple SerDes ports capable of supporting 400 Gbps Ethernet connections. Both of these I/O standards represent the fastest, most recent specifications for inter- and intra-system data communications used in data centers and myriad other FPGA-based applications.

Fast, High-Capacity Memory Storage

Speedster7t FPGAs are designed with multiple GDDR6 SDRAM ports. GDDR6 SDRAMs provide the fastest SDRAM access speeds with the lowest DRAM cost (per stored bit). Together, these characteristics make GDDR6 SDRAM interfaces the best choice for next-generation system designs. Members of the Speedster7t FPGA family support as many as eight independent GDDR6 memory ports.

Massive On-Chip Data Movement

With multiple high-speed PCIe Gen5 and 400 Gbps Ethernet ports combined with GDDR6 SDRAM interfaces, the Speedster7t FPGA family can move a tremendous amount of data directly between these various I/O ports and to the FPGA on-chip memory and computational resources. Speedster7t FPGAs employ both the familiar parallel interconnections of earlier FPGA generations and a new 2D network on chip (2D NoC) to facilitate the significantly

faster data transfer rates required by future data centers applications. The 2D NoC provides over 20 Tbps of data bandwidth within the FPGA device resources and I/O interfaces.

High-Speed, On-Chip Processing Resources

FPGAs excel at processing data at high-speeds due to their configurable logic and co-located SRAM resources. The Speedster7t FPGA family includes the same processing resources and memories found in previous generation FPGAs, but adds optimizations and new processing elements to further enhance performance for many applications, including AI/ML applications.

For example, Speedster7t FPGAs incorporate new resources called machine learning processor (MLP) blocks, which are large-scale, matrix-vector and matrix-matrix multiplication engines specifically designed to accelerate AI/ML applications. MLP blocks support fixed and floating-point computations and their resources are fracturable to support the wide range of numerical precision employed by AI/ML applications.

The MLP block architecture has been designed to exploit data reuse opportunities that are inherent to matrix-vector and matrix-matrix multiplication. This data reuse significantly reduces the amount of data movement among memories, which increases AI/ML algorithm performance while cutting power consumption. In addition, multipliers implemented with the Speedster7t FPGA lookup tables (LUTs) have been reformulated with the industry's most efficient modified Booth's algorithm, which doubles LUT-based multiplier performance for AI/ML algorithms.

Feature Summary

- Two-dimensional network on chip (2D NoC) enabling high bandwidth data flow throughout and between the FPGA fabric and hard I/O and memory controllers and interfaces
- MLP blocks with arrays of multipliers, adder trees, accumulators, and support for both fixed and floating point operations
- Multiple PCIe Gen5 ports
- High-speed SerDes transceivers, supporting 112 Gbps PAM4 and 56 Gbps PAM4/NRZ modulation, as well as lower data rates
- Hard Ethernet MACs that support up to 400 Gbps
- GDDR6 and DDR SDRAM controllers and interfaces (the Speedster AC7t1400 and AC7t1500 supports DDR4; the AC7t700 and AC7t800 supports both DDR4 and DDR5)
- New logic architecture with 6-input LUTs (6LUT), 8-bit ALUs, flip-flops, and a reformulated multiplier LUT (MLUT) mode based on a modified Booth's algorithm, which doubles the performance of LUT-based multiplication
- Fabric routing enhanced with dedicated bus routing and active bus muxing
- 72-kb BRAM and 2-kb LRAM memory blocks
- GPIO supporting multiple I/O standards
- PLLs to support multiple, on-chip clock domains
- Support for multiple types of programming interfaces, including configuration over PCIe.
- Partial reconfiguration of the FPGA fabric
- Remote update of the FPGA fabric
- Security features for encrypting and authenticating bitstreams
- Debug support through Achronix Snapshot

Family Features

Table 1 • Speedster7t FPGA Family Overview

Feature	AC7t700[1]	AC7t800	AC7t1400[1]	AC7t1500
Logic Density				
System Logic Cells (SLCs)	730k	730k	1,546k	1,546k
6-Input Look-Up Tables (LUTs)	326k	326k	692k	692k
Machine Learning Processors[2]				
32-bit (INT)[3]	864	864	2,560	2,560
16-bit (FP or TensorFlow bFloat)[4]	1,728	1,728	5,120	5,120
24-bit (FP)	1,728	1,728	5,120	5,120
16-bit (INT)	3,456	3,456	10,240	10,240
8-bit/6-bit (INT or FP)	13,824	13,824	40,960	40,960
4-bit (INT or Block FP)	27,648	27,648	81,920	81,920
On-Chip Memory				
Total Memory	86 Mb	86 Mb	195 Mb	195 Mb
Local RAM (LRAM) Blocks (2.3 kb)	864	864	2,560	2,560
Block RAM (BRAM) Blocks (72 kb)	1,152	1,152	2,560	2,560
High-Performance Interfaces				
112 Gbps SerDes	24	24	32	32
DDR4/5 Memory Channels	1 (DDR4/DDR5)	1 (DDR4/DDR5)	1 (DDR4)	1 (DDR4)
GDDR6 Memory Channels	6 (1.5 Tbps)	6 (1.5 Tbps)	16 (4 Tbps)	16 (4 Tbps)
PCIe (Gen5)	1 (×8)	1 (×16)	1 (×8)	2 (×8 and ×16)
Ethernet (10 Gbps to 400 Gbps)	8 lanes 400G (max)	8 lanes 2 × 400G (max)	16 lanes 400G (max)	16 lanes 2 × 400G (max)
Performance				
2D NoC bandwidth (Tbps)	12	12	21	21
ML TOps: INT-8 or bFloat-16[5]	20.5	20.5	61	61

Feature	AC7t700[1]	AC7t800	AC7t1400[1]	AC7t1500
Packaging				
42.5 × 42.5 mm BGA	1,677 balls	1,677 balls	–	–
52.5 × 52.5 mm BGA	–	–	2,597 balls	2,597 balls

Table Notes

1. AC7t700 and AC7t1400 SerDes total device bandwidth limited to < 500 Gbps
2. Resources per number format
3. INT – Integer
4. FP – Floating point
5. ML – Machine learning

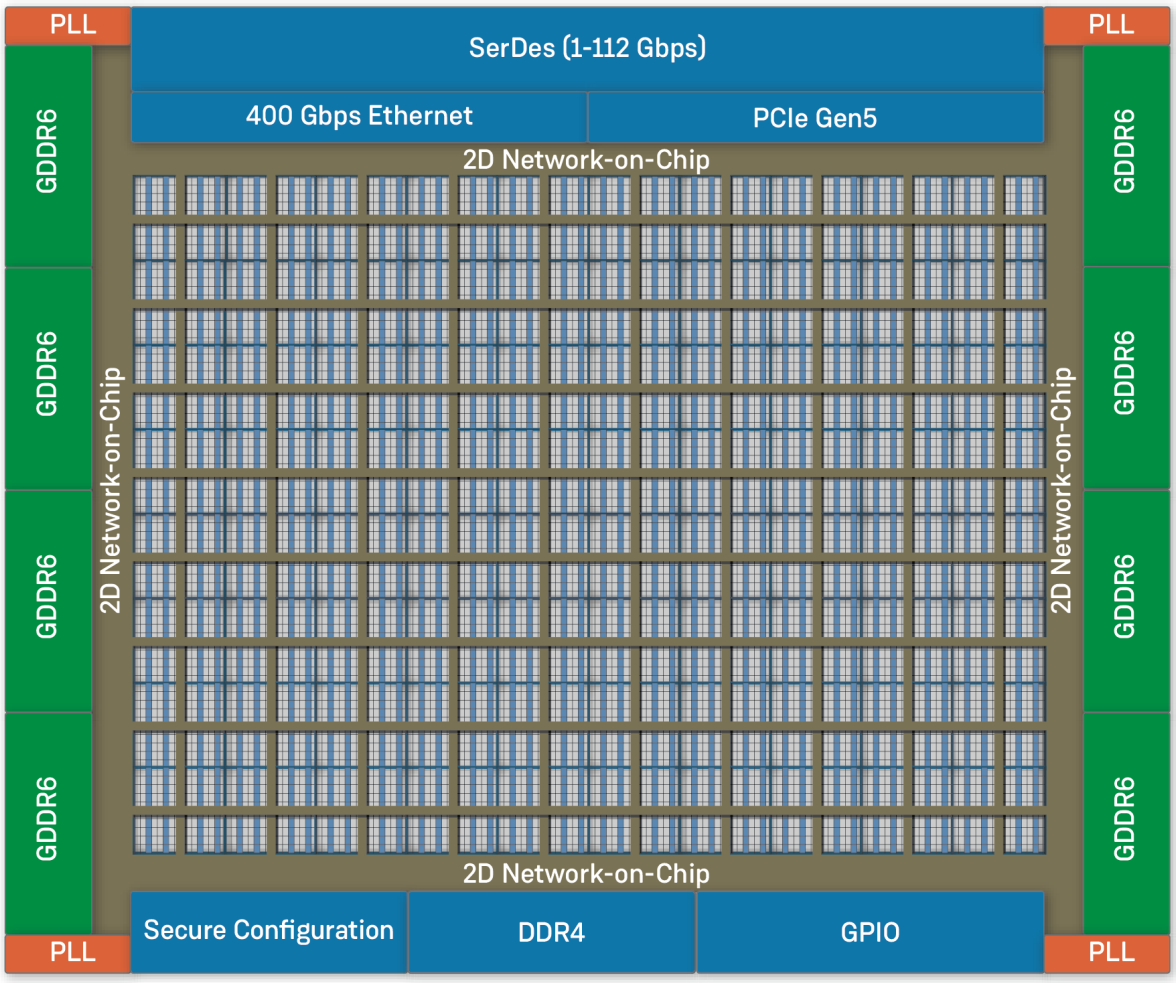

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Figure 1 • Speedster AC7t1400/AC71500 Top-Level Floorplan

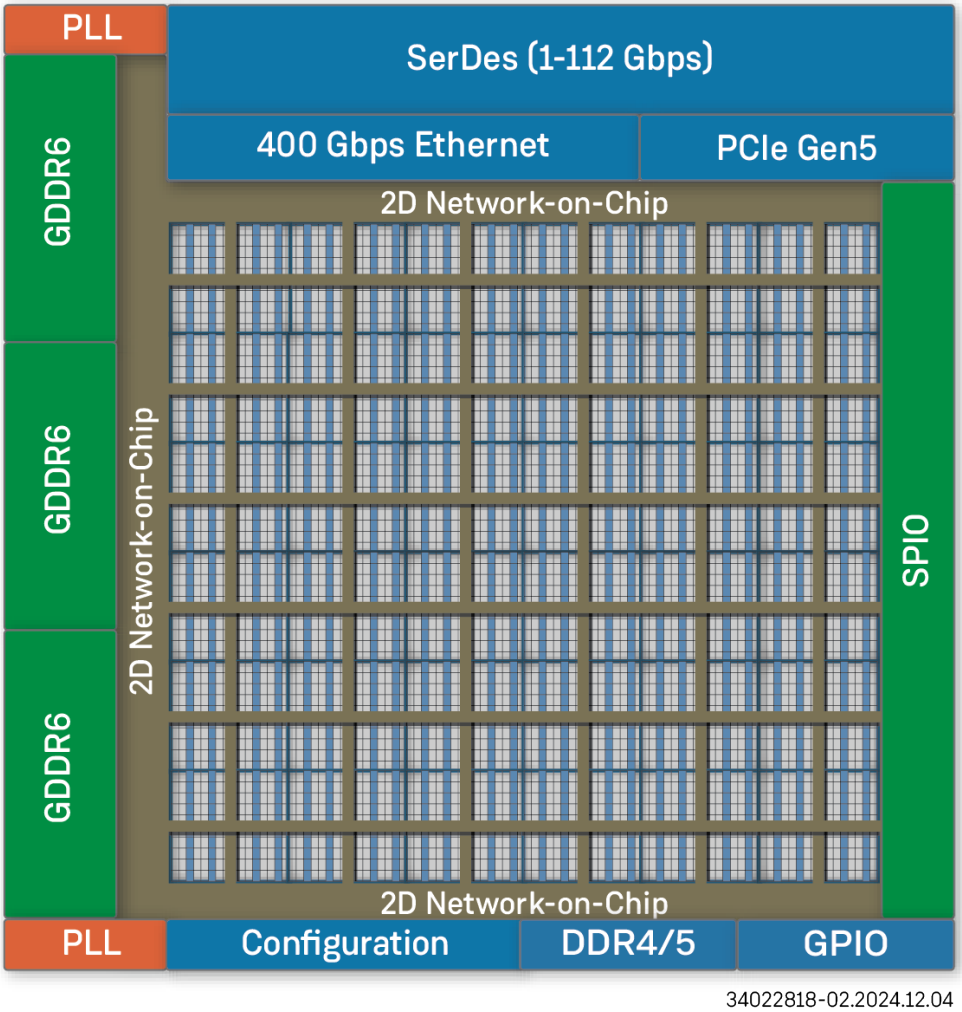


Figure 2 • Speedster AC7t700 AC7t800 Top-Level Floorplan

Chapter 2 : Speedster7t Fabric Architecture

The Speedster7t FPGA fabric is optimized for hardware acceleration, and is comprised of three main tile types:

- Reconfigurable logic blocks (RLBs) containing look-up tables, flip-flops, and ALUs
- Machine learning processor (MLP) blocks containing multipliers, adders, accumulators, and tightly-coupled memory (includes BRAM72k and LRAM2k)
- Standalone Block RAM 72k (BRAM72k) memory blocks (in the Speedster AC7t700/AC7t800)

The tiles are distributed as columns in the Speedster7t FPGA, and each tile consists of a routing switch box plus a logic block.

Fabric Clusters

Speedster7t FPGA fabric is constructed by arranging rows and columns of tiles into a basic unit of layout called a fabric cluster. The complete fabric in a device is created by replicating the fabric clusters into a larger grid of rows and columns. All fabric clusters are identical, containing exactly the same pattern of tile rows and columns, with a initiator and responder network access points (NAPs) in the center. The exact numbers of fabric clusters, the dimensions of each cluster, and the arrangement and types of tiles within each cluster, are specific per device. For example, the Speedster7t AC7t1400/AC7t1500 has 8 rows and 10 columns of fabric clusters, for a total of 80.

The following figure shows the fabric clusters:

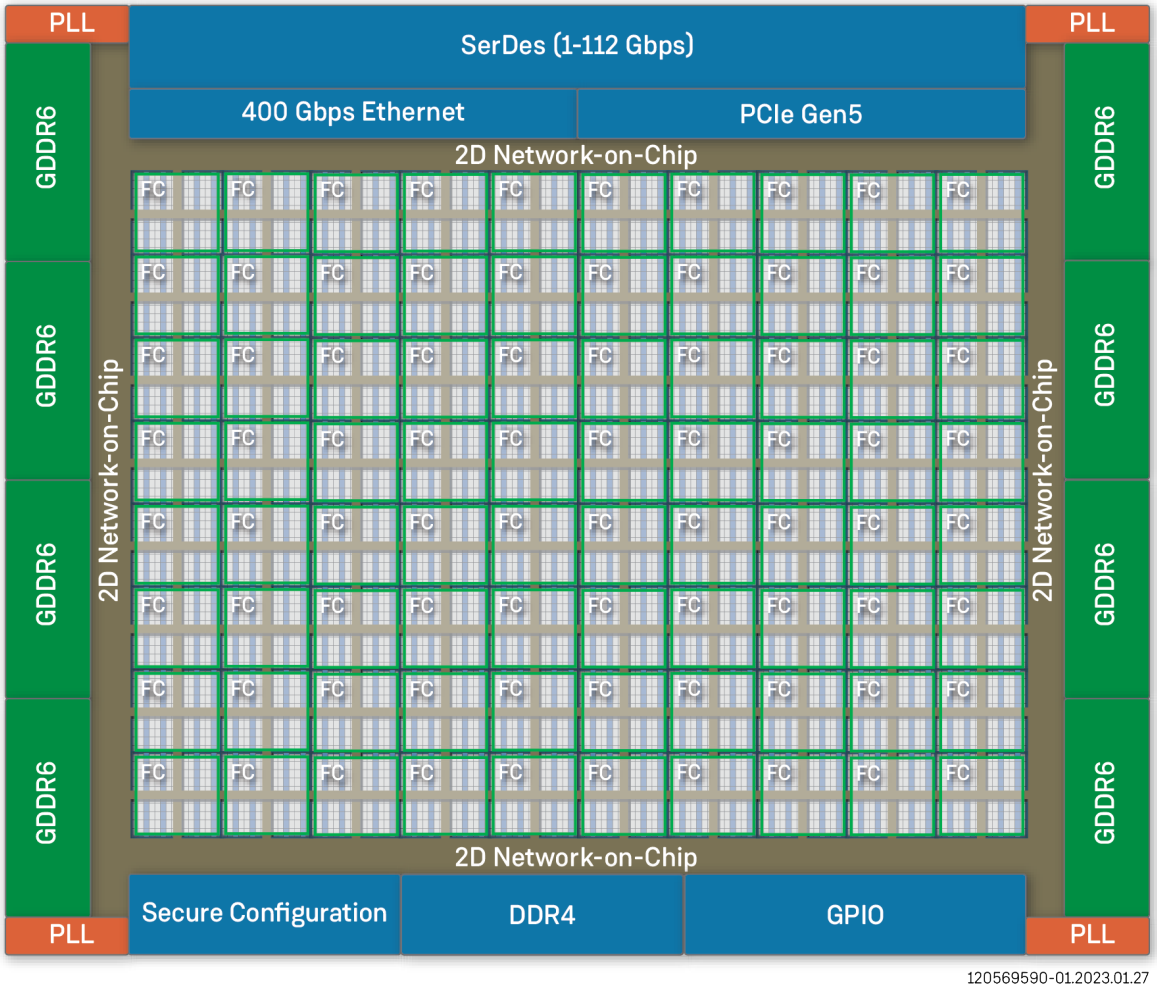


Figure 3 • Fabric Clusters on the Speedster AC7t1400/AC7t1500 FPGA

While fabric cluster boundaries are otherwise transparent to a user, a designer can make use of this regularity of fabric clusters if the design consists of a number of identical cores. If the cores are designed to fit within one or more fabric clusters, a complete design can be created by replicating that core multiple times across the device using the fabric cluster grid. Additionally, the fabric cluster structure along with the NAPs in the center of each cluster provide support for partial reconfiguration. The NAP provides a path to route signals on and off the NoC in the center of the cluster, and the regularity of the cluster makes it easy for multiple cores to be configured for the same cluster space.

Fabric Clock Network

Speedster7t FPGAs have two types of clock networks targeted to provide both a low-skew and a balanced architecture, as well as addressing the source-synchronous nature of data transfers with external interfaces:

1. The global clock network is the hierarchical network that feeds resources in the FPGA fabric. The global clock trunk runs vertically up and down the center of the core, sourced by global clock muxes at the top and bottom of the global trunk. The global clock network uses low-latency and low-skew distribution techniques to reach all possible endpoints in the FPGA fabric.
2. The interface clock network, available at the periphery of the fabric, facilitates the construction of interface logic within the FPGA fabric operating on the same clock domain as external logic. Specifically, interface clocks drive the logic that communicates with the hard IP interfaces on a Speedster7t FPGA. Interface clocks are optimized for low latency and drive logic within a specific area in the FPGA fabric.

Achronix provides dedicated clock dividers, glitchless clock switches, and clock gates for ease of use in a customer design. Additionally, ACE automatically provides support for inserting programmable delays at various points on a clock path to increase performance and easily facilitate timing closure.

Fabric Routing

Global Interconnect

All tiles in the fabric are connected through the global interconnect, allowing for routing between elements e.g., RLBs, MLPs, BRAMs, etc. Switchboxes in each tile act as the connection points between vertical and horizontal routing tracks. In addition to the traditional per-signal routing, the Speedster7t FPGA family introduces bus routing for high-performance data paths.

Bus Routing

The Speedster7t FPGA includes both traditional per-bit routing, as well as dedicated bus routing. The Speedster7t FPGA architecture includes separate dedicated bus-based routing for high-performance datapaths. These buses are placed into groups of up to 8 bits wide and are routed independently from standard routing in order to significantly reduce congestion.

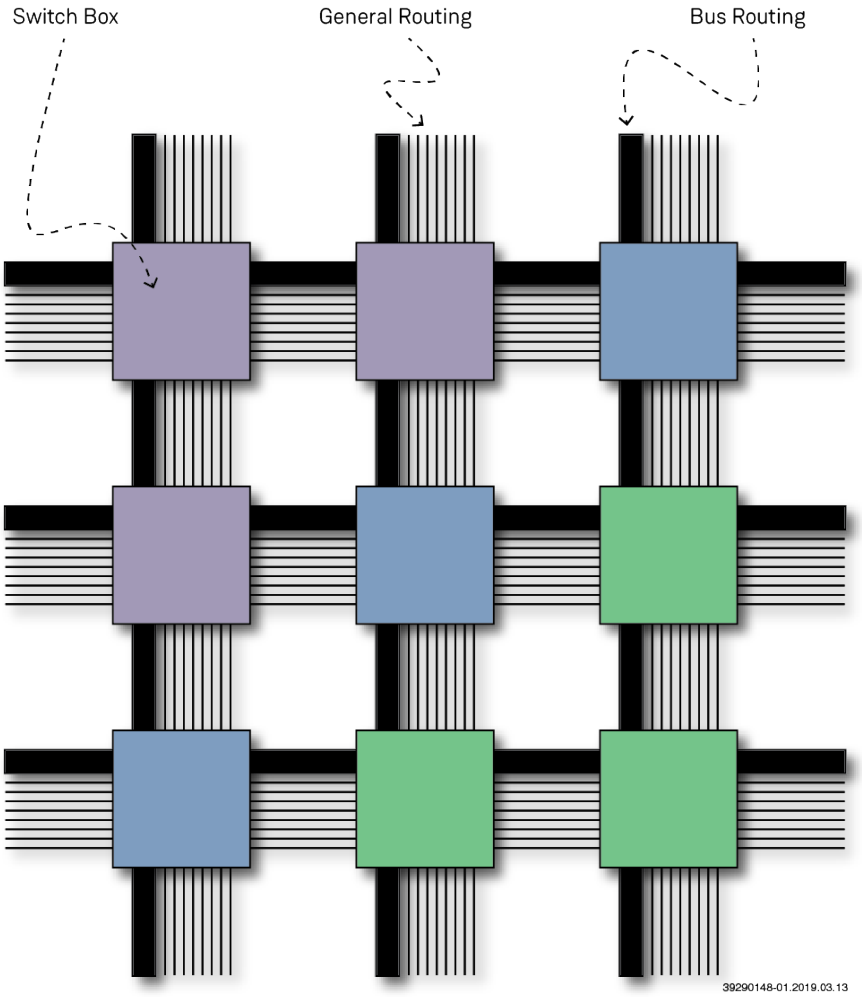


Figure 4 • Speedster7t Bus Routing

Additionally, the Speedster7t FPGA architecture introduces a programmable switch network for bus routing. Four 8-bit buses, one from each direction, enter each Speedster7t switchbox. There is a 4 × 1 MUX driving each of the 8-bit buses inside the switchbox — three from other sides and one from the local logic block.. These bus MUXes are cascadable for wider muxing requirements. This added muxing reduces overall logic and routing resources for a design, leading to improved performance and smaller area.

Reconfigurable Logic Block (RLB)

An RLB contains 6-input look-up-tables (LUT6), a number of registers, and 8-bit fast arithmetic logic units (ALU8). The following table provides information on the resource counts inside an RLB.

Table 2 • RLB Resource Counts

Resource	Count
LUT6	12
Registers	24
8-bit ALU	3

The following features are available using the resources in the RLB:

- 8-bit ALU for adders, counters, and comparators
- 8-to-1 MUX with single-level delay (can be inferred)
- Support for LUT chaining within the same RLB and between RLBs
- Dedicated connections for high-efficiency shift registers
- Multiplier LUT (MLUT) mode for efficient multipliers (for Speedster7t devices only)
- Ability to fan-out a clock enable or reset signal to multiple tiles without using general routing resources
- 6-input LUT configurable to function as two 5-input LUTs using shared inputs and two outputs
- Support for combining two 6-input LUTs with a dynamic select to provide 7-input LUT functionality

MLUT Mode

The RLB includes an MLUT mode for an efficient LUT-based multiplication. MLUT mode results in 2 × 2 multiplier building blocks that can be stacked horizontally and vertically to generate any size signed multiplier. For example, a 2 × 4 multiplier building block can be generated with two LUT6s, and one RLB can perform a 6 × 8 multiply.

> **Note**
> MLUT mode is supported by the MLUT generator within ACE to help build the desired multiplier.

Machine Learning Processor (MLP) Block

The machine learning processor block (MLP) is an array of up to 32 multipliers, followed by an adder tree, and an accumulator. The MLP is also tightly coupled with two memory blocks, a BRAM72k and LRAM2k. These memories can be used individually or in conjunction with the array of multipliers. The number of multipliers available varies with the bit width of each operand and the total width of input data. When the MLP is used in conjunction with a BRAM72k, the number of data inputs to the MLP block increases, enabling the use of additional multipliers.

The MLP offers a range of features:

- Configurable multiply precision and multiplier count. Any of the following modes are available:
  - Up to 32 multiplies for 4-bit integers or 4-bit block floating-point values in a single MLP
  - Up to 16 multiplies for 8-bit integers or 8-bit block floating-point values in a single MLP
  - Up to 4 multiplies for 16-bit integers or 16-bit block floating-point values in a single MLP
  - One multiplier for 32-bit integers in a single MLP
  - Up to 2 multiplies for 16-bit floating point with both 5-bit and 8-bit exponents in a single MLP
  - Up to 2 multiplies for 24-bit floating point in a single MLP
- Multiple number formats:
  - Integer
  - Floating point 16 (IEEE half-precision and TensorFlow bfloat16 formats)
  - Floating point 24
  - Block floating point, a method that combines the efficiency of the integer multiplier-adder tree with the range of the floating point accumulators
- Adder tree and accumulator block
- Tightly-coupled register file (LRAM) with an optional sequence controller for easily caching and feeding back results
- Tightly-coupled BRAM for reusable input data such as kernels or weights
- Cascade paths up a column of MLPs
  - Allows for broadcast of operands up a column of MLPs without using up critical routing resources
  - Allows for adder trees to extend across multiple MLPs
  - Broadcast read/write to tightly-coupled BRAMs up a column of MLPs to efficiently create large memories

Along with the numerous multiply configurations, the MLP block includes optional input and pipelining registers at various locations to support high-frequency designs. There is a deep adder tree after the multipliers with the option to bypass the adders and output the multiplier products directly. In addition, a feedback path allows for accumulation within the MLP block.

The following block diagrams show the MLP using the fixed or floating-point formats:

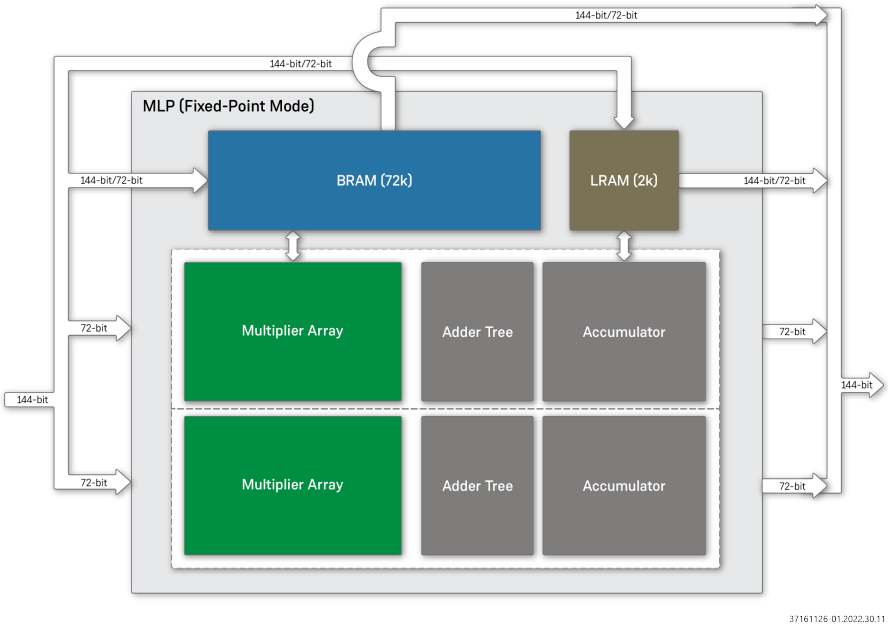


Figure 5 • MLP Using Fixed-Point Mode

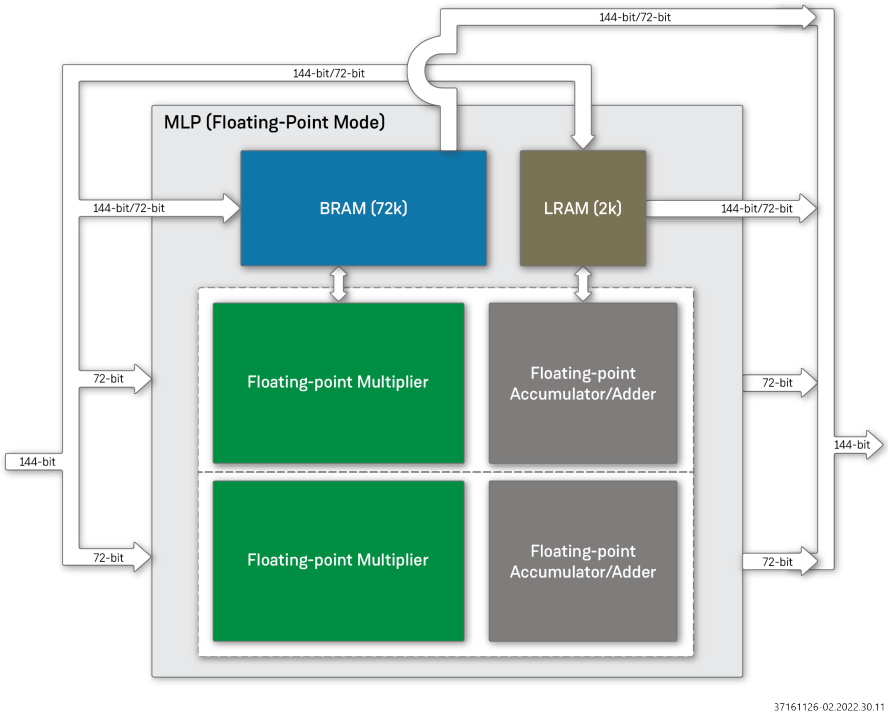


Figure 6 • MLP Using Floating-Point Mode

A powerful feature available in the Achronix MLP is the ability to connect several MLPs with dedicated high-speed cascade paths. The cascade paths allow for the adder tree to extend across multiple MLP blocks in a column without using extra fabric routing resources, and a data cascade/broadcast path is available to send operands across multiple MLP blocks. Cascading input or result data to multiple MLPs in parallel allows for complex, multi-element operations to be performed efficiently without the need for extra routing. The following diagram shows the cascade paths across MLPs:

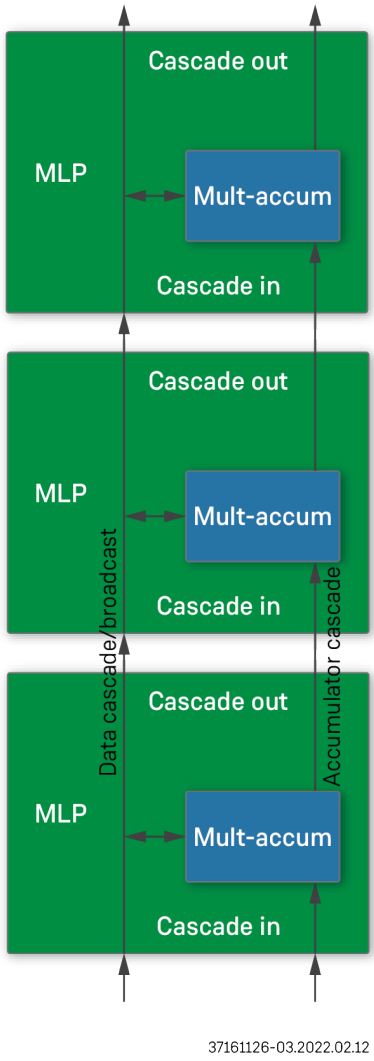


Figure 7 • MLP Cascade Path

Block RAM 72k (BRAM72k)

The BRAM72K primitive implements a 72Kb simple-dual-port (SDP) memory block with one write port and one read port. Each port can be independently configured with respect to size and function, and can use independent read and write clocks. The BRAM72K can be configured as a simple dual port or ROM memory. The key features (per block RAM) are summarized in the following table:

Table 3 • BRAM72K Key Features

Feature	Value
Block RAM size	72Kb
Organization	512 × 144, 128 × 512, 1024 × 72, 1024 × 64, 2048 × 36, 2048 × 32, 4096 × 18, 4096 × 16, 8192 × 9, 8192 × 8, or 16384 × 4
Physical Implementation	Columns throughout device
Number of Ports	Simple Dual Port (independent read and write)
Port Access	Synchronous writes, synchronous reads (write and read clocks can be asynchronous to each other)
FIFO	Built-in FIFO controller with dedicated pointer and flag circuitry

The BRAM72K ports are Illustrated in the following figure:

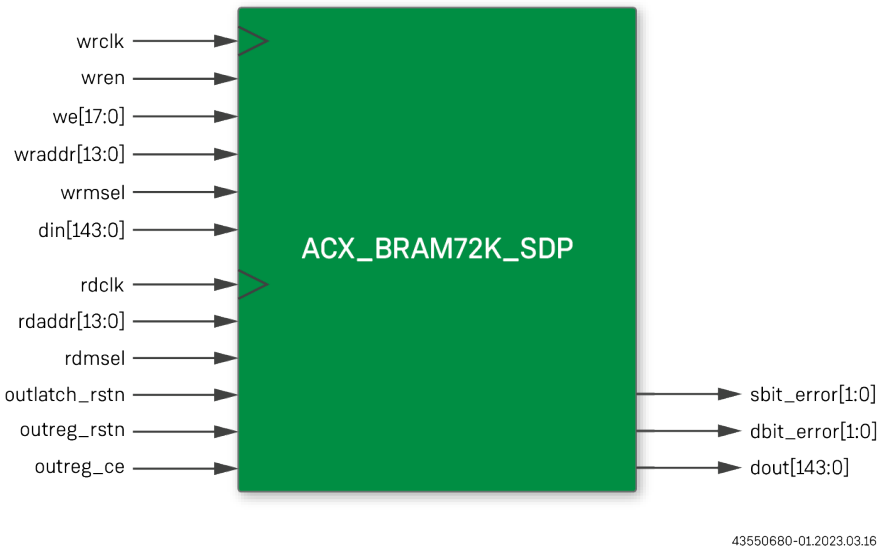


Figure 8 • BRAM72K Block Diagram

Local RAM 2k (LRAM2k)

The LRAM2K implements a 2,304-bit memory block configured as a 32 × 72 simple dual-port (one write port, one read port) RAM. The LRAM2K has a synchronous write port. The read port is configured for asynchronous read operations with an optional output register. A summary of LRAM2K features is shown in the following table:

Table 4 • LRAM2K Key Features

Feature	Value
Local RAM size	2,304 bits
Organization	16 × 144, 32 × 72 or 64 × 36 (depth × width)
Physical Implementation	Columns throughout device
Number of Ports	Simple dual port (one read, one write)
Port access	Synchronous writes, combinatorial reads
FIFO	Built-in FIFO controller with dedicated pointer and flag circuitry

The LRAM2K ports are shown in the following figure:

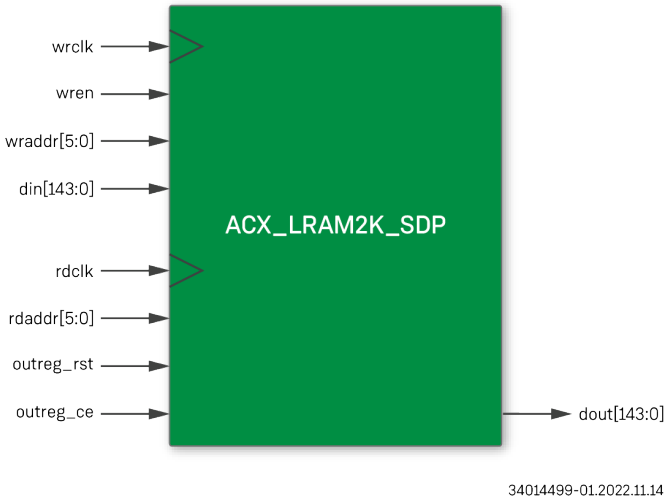


Figure 9 • LRAM2K Block Diagram

Chapter 3 : Speedster7t PLLs

The AC7t1400 and AC7t1500 devices host sixteen general-purpose PLLs, four in each corner of the FPGA; whereas, the Speedster AC7t700/AC7t800 devices host eight PLLs on the southwest and northwest corners of the FPGA. They are fractional-N divide, spread-spectrum PLLs, supporting a wide range of frequencies with excellent jitter performance. The general-purpose PLLs can be used to drive low-skew, high-speed clocks to nearby I/O, the global clock network, and interface clocks in the FPGA fabric.

Available features in the PLLs are:

- Programmable PLL with fractional-N divide and spread-spectrum clock generation
- Wide range of output frequencies supported: 7.5 MHz to 2 GHz
- Reference clock from dedicated clock I/O, adjacent PLLs (for cascading PLLs), as well as PLLs from other device corners
- Up to four output clocks
- Reference clock and output clock dividers
- Inner and outer bypass paths
- Output duty cycle 50%
- Low jitter
- Low power

Table 5 • PLL Details

Parameter	Min	Max	Units
Reference frequency	5	600	MHz
Output frequency	7.5	2000	MHz
Maximum long-term jitter	±1% divided reference clock		

Chapter 4 : Speedster7t FPGA I/O and PHY

Speedster7t FPGAs have a variety of I/O and PHY to communicate with external components.

112 Gbps SerDes

Speedster7t FPGAs provide high-speed serial transceivers (SerDes) which can be used for interface protocols running from 1 Gbps up to 112 Gbps. The SerDes are designed to support NRZ and PAM4. The maximum rate is 56 Gbps NRZ and 112 Gbps PAM4. The Speedster7t FPGA provides a PCS and PMA to support the needs of many common high-speed serial protocols.

PMA Features

- Data rates from 1 Gbps to 112.5 Gbps
- Supports data path widths to the fabric of 16, 20, 32, 40, 64, and 128 bits (not all data widths are supported at all data rates)
- DC coupling or external AC coupling
- Support for oversampling
- BIST with near/far-end loopback and PRBS 7, 13, 15, 23, 31 generator/checker
- Eye monitor

PCS Features

- The Ethernet subsystem supports data rates from 10 Gbps to 400 Gbps (400G × 4 where the SerDes rate is 106.3 Gbps)
- The raw SerDes Gearbox Mode supports 1 Gbps to 112.5 Gbps
  - Support for 67b/64b gearbox in synchronous mode
  - Support for 66b/64b CAUI gearbox in both synchronous and asynchronous mode
  - Native support for Ethernet 10G/25G/50G/100G, XAUI, CPRI, Jesd4C, SyncE, and Interlaken
- The PCIe subsystem supports ×1, ×4, ×8 or ×16 widths in Gen1, Gen2, Gen3, Gen4 and Gen5 link speeds
- The raw SerDes Pipe Mode is PIPE5.1 compliant for PCIe
  - 8b/10b encoding/decoding support for PCIe 40-bit internal data paths
  - Comma detection and byte/word alignment for PCIe 8b/10b
  - 128b/130b encoding/decoding support for PCIe Gen3/Gen4/Gen5 32-bit internal data path
- Bypass mode for PCS (bypasses the PCS)

GPIO Bank Configurations

Speedster7t architecture provides general-purpose I/O (GPIO) pins to enable communication with external components, organized into two type of banks:

- The GPIO bank – GPIO banks have built-in features such as un-registered I/O, registered I/O, DDR mode, and SerDes mode, offering more options than traditional GPIO.
- The simple I/O bank – Simple I/O banks are closer to traditional GPIO and do not include the registered I/O, DDR mode, or SerDes mode features.

> **Note**
>
> Speedster7t AC7t1400/AC7t1500 FPGAs only have the GPIO Bank, while AC7t700/AC7t800 FPGAs have both GPIO and simple I/O banks.

GPIO DLLs

In each GPIO bank of the Speedster7t FPGAs, there are DLLs to support shifting of GPIO outputs. These programmable DLLs provide precise phase alignment between output signals, and include features such as:

- 256 taps
- Lock detection
- Power-down mode when not used in the design
- Control and status register read back

GPIO Electrical Standards

Speedster7t GPIOs support multiple I/O standards at multiple voltages. The following table lists the supported I/O standards available in single-ended or differential configuration. The next section describes separate clock I/O banks.

Table 6 • Supported General-purpose I/O Standards

Supported I/O Standard	Supported Voltage (V)
HSTL Class I	1.8
HSUL	1.2
LVCMOS	1.1
	1.2
	1.35
	1.5
	1.8

Supported I/O Standard	Supported Voltage (V)
SSTL Class I	1.2
	1.35
	1.5
	1.8
SSTL Class II	1.8

Special-Purpose I/O (SPIO)

In the DDR5/DDR4 memory subsystem, the controller can be bypassed, such that I/O pins can be used for purposes other than DDR memories. In bypass mode, DDR I/O can be used as special-purpose I/O, similar to GPIO, but limited to the DDR 1.2V electrical standard to support low-frequency interfaces running at up to 100 Mhz.

Clock I/O

Speedster7t FPGAs provide two types of clock I/O pins to enable communication with external components:

- Multi-standard I/O (MSIO) – clock I/O that support multiple I/O standards at multiple voltages, including pseudo-differential.
- Reference clock differential I/O (REFIO) – clock I/O that support LVCMOS, LVDS, and LVPECL.

The following table lists the supported I/O standards for each clock I/O type.

Table 7 • Supported Clock I/O Standards

I/O Standard Supported	Supported Voltage (V)	Single-Ended/Differential
MSIO		
HSTL Class I	1.5	single-ended, differential
	1.8	
HSTL Class II	1.5	
LVCMOS	1.5	
	1.8	
SSTL Class I	1.5	
	1.8	
SSTL Class II	1.8	

I/O Standard Supported	Supported Voltage (V)	Single-Ended/Differential
REFIO		
LVCMOS	1.5	single-ended, differential
	1.8	
LVDS	1.5	differential
	1.8	
LVPECL	1.5	
	1.8	

Chapter 5 : Speedster7t FPGA Two-Dimensional Network on Chip

The Speedster7t family of FPGAs has a network that enables extremely high-speed data flow between the FPGA core and the interfaces around the periphery as well as between logic within the FPGA itself. This on-chip network supports a cross-sectional bidirectional bandwidth exceeding 20 Tbps. It supports a multitude of interface protocols including GDDR6, DDR4/5, 400G Ethernet, and PCI Express data streams while greatly simplifying access to memory and high-speed protocols. The Achronix two-dimensional network on chip (2D NoC) provides for read/write transactions throughout the device as well as specialized support for 400G Ethernet streams in selected columns.

Initiator Endpoints

- 80 2D NoC access points (NAPs) on the AC7t1400/AC7t1500; 36 NAPs on the AC7t700/AC7t800
- Initiators connected to the 2D NoC include:
  - NAPs distributed throughout the FPGA core
  - All PCI Express Interfaces
  - FPGA configuration unit (FCU)

Responder Endpoints

- 80 2D NoC access points (NAPs) on the AC7t1400/AC7t1500; 36 NAPs on the AC7t700/AC7t800
- Any initiator on the 2D Noc can access the following responders:
  - NAPs distributed throughout the FPGA core
  - 16x GDDR6 memory interfaces
  - DDR4/5 interface
  - All PCI Express Interfaces
  - All control and status register (CSR) interfaces of all subsystem cores
  - The FCU (enables configuring of FPGA and interface subsystems)

Packet Endpoints

- 80 vertical NAP packet interfaces on AC7t1400/AC7t1500 devices (36 vertical NAP packet interfaces on AC7t700/AC7t800 devices), distributed throughout the FPGA core for fabric-to-fabric streams
- 80 horizontal NAP packet interfaces on AC7t1400/AC7t1500 devices (36 horizontal NAP packet interfaces on AC7t700/AC7t800 devices), distributed throughout the FPGA core for fabric-to-fabric streams
- 32 of the 80 vertical NAPs on AC7t1400/AC7t1500 and 12 of the 36 vertical NAPs on AC7t700/AC7t800 can send and receive data to/from the Ethernet subsystems; each Ethernet controller connects to two dedicated 2D NoC columns

- Two Ethernet subsystems for AC7t1400/AC7t1500. One Ethernet subsystems for AC7t700/AC7t800. These subsystems support a mix of up to 4× 400 Gbps Ethernet or 16× 100 Gbps Ethernet

2D NoC Features

The 2D NoC provides a method to easily connect high-bandwidth interfaces to the FPGA fabric, as well as enabling communication between memory and high-speed protocols. To make these high-bandwidth connections both flexible and easy to use, the 2D NoC provides the following features.

Table 8 • 2D NoC Features

Feature Summary	Feature Description
2D NoC Interface Modes	The 2D NoC-to-FPGA access point (NAP) supports the following modes: • AXI 256b responder mode • AXI 256b initiator mode • Ethernet mode • NAP-to-NAP data streaming mode
2D NoC Address Decoding	The 2D NoC has a global address map and handles all address decoding on transactions, making it easy to send transactions from one endpoint to another.
2D NoC Memory Address translation and Firewall	The 2D NoC implements an address translation table for each NAP. This table allows the FPGA design to control how the global memory space is arranged for each NAP, and allows access to specific memory regions to be blocked for security, also on a per-NAP basis.
2D NoC Forwarding Latency	1 to 3.5 ns of latency from one NAP to the next on the same row or column respectively.
2D NoC Flow Control	The 2D NoC manages flow control internally, such that data is never dropped. Priority NAP weights may be configured to regulate the flow control which affects congestion and latency.

The 2D NoC extends both vertically and horizontally until reaching the edges of the device. The following diagram shows the Speedster AC7t1400/AC7t1500 connections between the peripheral portion of the 2D NoC, the high-bandwidth interfaces, and the columns and rows of the 2D NoC. As shown, the Ethernet has dedicated connections of up to 400G to specific columns of the 2D NoC. The PCIe ×16 and ×8 connect to the periphery of the 2D NoC at 512 Gbps and 256 Gbps respectively. For GDDR6, the 2D NoC can achieve bandwidth of up to 2 Tbps over the full group of GDDR6 interfaces on each side of the FPGA. The columns and rows of the 2D NoC can move traffic to/from the user logic in the fabric at up to 512 Gbps in each direction.

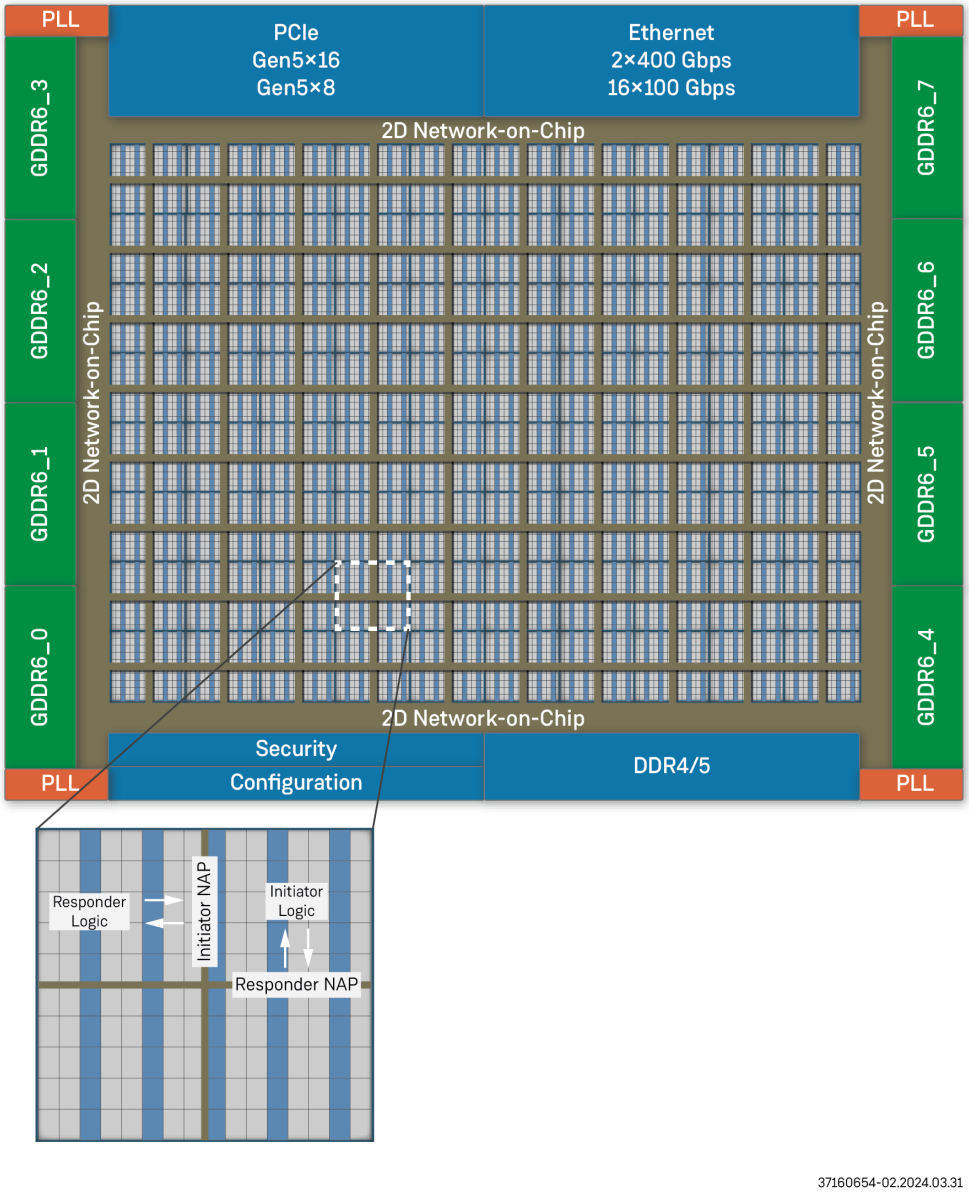


Figure 10 • Speedster AC7t1400/AC7t1500 2D NoC Showing Initiator and Responder Endpoints

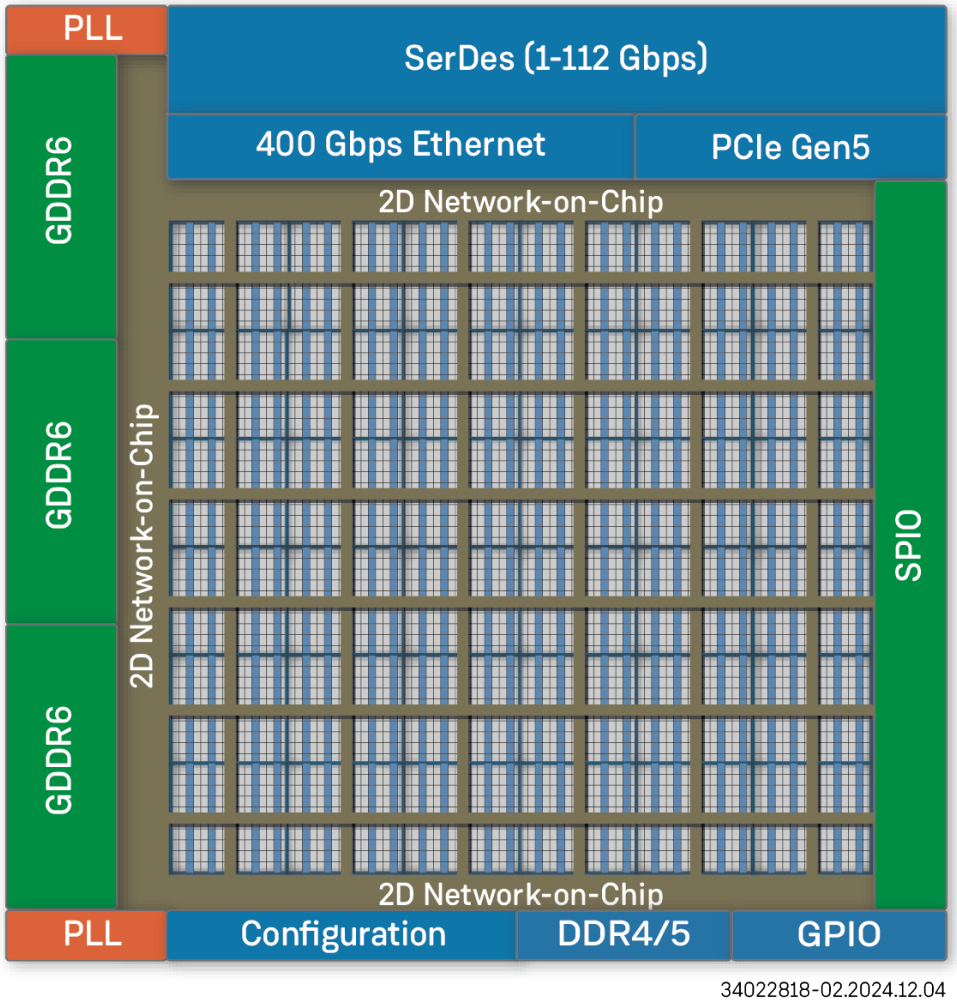


Figure 11 • Speedster AC7t700/AC7t800 2D NoC

Columns and Rows of the 2D NoC

The 2D NoC is composed of regularly-spaced node elements at the center of each cluster throughout the core fabric of the FPGA. The 2D NoC nodes provide connectivity to adjacent nodes in both the horizontal and vertical directions. Each horizontal and vertical link within the 2D NoC supports 512 Gbps throughput in both directions.

The 2D NoC transaction mapping logic is optimized for AXI read and write transactions. User initiator logic implemented in the FPGA core can issue AXI read or write transactions to the NAP AXI responder, and the 2D NoC row carries the transaction to the east or west boundary of the FPGA core to be issued to the deep DDR4/5 memory interface or one of the high-speed GDDR6 memory interfaces. PCIe transactions arriving from the north side of the device are issued to the 2D NoC columns, which transport the transaction requests down the columns to user responder logic in the FPGA.

Each row and column can support a full 512 Gbps of traffic.

The rows and columns of the 2D NoC support both transactional and non-transactional data transfers such as streams of data.

- **Transactional data transfer** – this type of transfer includes AXI read and write commands, data, and responses. The command transfers are typically a single cycle, and data transfers are typically one or more cycles, depending on the length of the burst.
- **Non-transactional data transfer** – this type of transfer pushes data streams through the 2D NoC as in a FIFO. A point-to-point data transfer, it is used in two types of transfers:
  - **Ethernet** – this transfer allows data to be bundled as longer streams of data. Data is sent down selected columns from Ethernet to a specific NAP on the column.
  - **NAP-to-NAP** – the 2D NoC allows the sending of data between NAPs within the same column or the same row. In this mode, streams of data are transferred from endpoint to endpoint without further processing.

Peripheral 2D NoC

The peripheral portion of the 2D NoC carries transactions between the FPGA core and the peripheral IP blocks, as well as from NAP-to-NAP when using AXI mode. The 2D NoC can also carry transactions directly between the different peripheral IP blocks. The 2D NoC provides the following services:

- Address decoding
- Transaction command and response routing
- Width adaptation
- Frequency adaptation (clock domain crossing)
- Burst adaptation
- Protocol conversion (e.g., AXI to/from APB)

The peripheral portion of the 2D NoC only carries read and write transactions. It does not carry Ethernet packets or data from the SerDes.

Each row of the 2D NoC presents an AXI initiator to the periphery of the 2D NoC on both the west and east side of the Speedster AC7t1500, and to the west side of the AC7t800. Each column of the 2D NoC presents an AXI responder to the periphery of the 2D NoC on the north side of the FPGA. This structure allows user logic to read or write any external IP or control and status register (CSR) interface and allows any external IP with an initiator interface to access any responder endpoints with attached user logic.

The Speedster7t FPGA 2D NoC has two important features:

- The 2D NoC is usable immediately when reset is released, without configuration of any control and status registers, the FPGA fabric, or the IP interfaces.
- The 2D NoC supports transfers between IP cores (such as PCIe and GDDR6) without requiring the FPGA fabric to be configured.

Connectivity Between 2D NoC and Endpoints on FPGA

The connectivity between the 2D NoC and the different endpoints on the FPGA device can be categorized into three scenarios: 2D NoC-to-user logic connectivity, 2D NoC-to-interface IP connectivity, and 2D NoC-to-FCU connectivity.

2D NoC-to-User Logic Connectivity

A 2D NoC access point (NAP) must be instantiated in the user design in order to gain access to the rows and columns of the 2D NoC. There is a 2D NoC column with an initiator NAP and a responder NAP in each cluster. To the FPGA core, these access points look like any other logic columns in the FPGA fabric. The FPGA core provides a clock to the NAP as it does for any other column type. Internally, the NAP has an asynchronous FIFO used to adapt the data rates to what the FPGA can achieve.

2D NoC-to-Interface IP Connectivity

The 2D NoC enables any 2D NoC access point in the FPGA to access any interface IP responder, including any of the GDDR6 AXI interfaces and any of the DDR4/5 or PCIe controllers. It is also feasible to access the control and status interfaces of every IP core, DLL/PLL, and the FCU, through the 2D NoC.

DDR4/5 and GDDR6 Connectivity

Each memory interface presents a 256-bit responder interface to the 2D NoC and accepts read or write transactions. Multiple 2D NoC access points can issue transactions to a single memory interface to utilize the full bandwidth provided by the high-speed memory interfaces.

PCI Express Connectivity

The PCIe IP AXI interface is connected directly to the 2D NoC.

2D NoC-to-FCU Connectivity

The FPGA configuration unit (FCU) can issue transactions to the 2D NoC, allowing the configuration logic to set any CSR interface on the device. Initiators on the 2D NoC, such as FPGA logic and the PCIe IP AXI initiator can issue commands to the FCU, allowing for configuration over PCIe and other useful features.

For additional information on the NoC please refer to the ***Speedster7t 2D Network on Chip User Guide*** UG089[1].

1 https://www.achronix.com/documentation/speedster7t-2d-network-chip-user-guide-ug089

Chapter 6 : Speedster7t FPGA Interface Subsystems

Speedster7t FPGAs have dedicated, hard interfaces to support the latest and most advanced versions of serial and memory interfaces used in high-performance networking and compute offload applications including 400G Ethernet, PCI Express Gen5, GDDR6, and DDR4 or DDR5. The combined interfaces achieve up to 8.4 terabits per second of total device bandwidth.

Ethernet

Speedster7t FPGAs include one or more Ethernet subsystems consisting of up to 8 SerDes lanes and multiple Ethernet MACs. The Ethernet MACs are very flexible and can support multiple ports up to 400G, with each SerDes lane able to achieve a line rate between 10G and 100G. The Ethernet subsystem connects to the FPGA fabric through the two-dimensional network on chip (2D NoC). The following table lists the supported Ethernet modes for all devices.

Table 9 • Supported Ethernet Modes

Mode	Connection	AC7t700/AC7t800	AC7t1400/AC7t1500
400GAUI-4	4 × 100G	✓	✓
400GBASE-CR4		✓	✓ (1)
400GBASE-CR8	8 × 50G	✓	✓
400GAUI-8		✓	✓
200GBASE-CR2	2 × 100G	✓	✓ (1)
200GAUI-2		✓	✓
200GBASE-CR4	4 × 50G	✓	✓
200GAUI-4		✓	✓
100GAUI-1	1 × 100G	✓	✓
100GBASE-CR1		✓ (2)	✓ (1, 2)
100GBASE-CR2	2 × 50G	✓	✓
100GBASE-CR4	4 × 25G	✓	✓
50GBASE-CR2	2 × 25G	✓	✓

Mode	Connection	AC7t700/AC7t800	AC7t1400/AC7t1500
25GBASE-CR1	1 × 25G	✓	✓
25GAUI-1		✓	✓
10GBASE-CR1	1 x 10G	✓	✓
XFI		✓	✓

Table Notes

1. Without ANLT.
2. Without RS-FEC-Interleaved.

Additionally, the supported modes depend on the device's speed grade. For information on the speed grade, number of Ethernet subsystems available in a device, and required SerDes lanes for each mode, refer to the ***Speedster7t Ethernet User Guide*** (UG097)[2].

PCI Express

Speedster7t FPGAs have up to two PCIe interfaces. One interface supports up to 16 lanes (×16). Some Speedster7t FPGAs have a second PCIe interface that supports up to 8 lanes (×8). Both PCIe controller interfaces support operation as either an endpoint or as a root complex. Both PCIe interfaces connect to the FPGA fabric through the two-dimensional network on chip (2D NoC) up to Gen5.For information on the number of PCIe subsystems available in a device, refer to the table, Speedster7t Family Overview (page 3).

Table 10 • Speedster7t FPGA PCIe Interface Specifications

Feature	AC7t700/AT7t800	AC7t1400/AC7t1500	
	PCIe Port 1	PCIe Port 0	PCIe Port 1
PCI Express Specification	Revision 5.0, Version 0.9		
PIPE	Version 5.1.1		
Maximum Speed	Gen5		
Maximum width(†)	×16	×8	×16
Maximum throughput(†)	512 GTs(†)	256 GTs	512 GTs(†)

2 https://www.achronix.com/documentation/speedster7t-ethernet-user-guide-ug097

Feature	AC7t700/AT7t800	AC7t1400/AC7t1500	
	PCIe Port 1	PCIe Port 0	PCIe Port 1
Supported functionality	Root-Port + End-Point	Root-Port + End-Point	Root-Port + End-Point
Maximum Speed	Gen5	Gen5	
DMA support	Yes	Yes	
DMA read channels	4	2	4
DMA write channels	4	2	4
Virtual channels	1	1	
Physical functions	4	2	4
SRIOV/Virtual functions	256	0	256
Advanced error reporting (AER) support	Yes	Yes	

Table Note

† The AC7t700 and AC7t1400 devices are limited to less than 500 Gbps total throughput across all serial interfaces.

GDDR6

Speedster7t FPGAs contain GDDR6 subsystems on the west and east sides to provide external high-bandwidth memory interface support. The controller and PHY implementation are compliant with the JEDEC GDDR6 SGRAM Standard JESD250. See the following table for a summary of the key specs and features.

Each GDDR6 interface has two channels, each of which can be enabled independently. The controller supports a wide range of features, including bus utilization optimization, page-hit mitigation, multiport front end (MPFE), reordering and error interrupt.

The GDDR6 subsystems can run up to a data rate of 16 Gbps with device densities from 8 Gb to 16 Gb. The implementation supports GDDR6 up to ×16 in non-clamshell modes and up to ×8 in clamshell modes. For information on the number of GDDR6 subsystems available in a device, see the Speedster7t Family Overview (page 3) table.

The GDDR6 controllers connect to the other interface subsystems on the Speedster7t FPGAs via the 2D NoC.

In AC7t1400/AC7t1500 devices, the GDDR6 subsystems can connect directly to the FPGA fabric via an AXI interface with support for full or half-rate clocking. The FPGA fabric and other subsystems can connect to GDDR6 in the following ways:

- A 256-bit AXI interface to the 2D NoC, which can run up to 1 GHz and connects to interface subsystems and FPGA fabric
- A 512-bit AXI direct-to-fabric interface, which can run up to 500 MHz (not available for AC7t700/AC7t800)

The PHY ZQ calibration can be configured as Initiator/Responder mode across multiple PHYs.

Furthermore, the IP comes with a memory test and analyzer core to enable standalone testing of the controller and memory during board bring up.

Table 11 • GDDR6 Key Specs and Features on Speedster7t FPGAs

GDDR6 Feature	Support in Speedster7t AC7t700/AC7t800 FPGAs	Support in Speedster7t AC7t1400/AC7t1500 FPGAs
Memory suppliers	Micron, Samsung, SK Hynix	Micron, Samsung, SK Hynix
Maximum number of memory devices per FPGA	6 (clamshell), 3 (non-clamshell)	16 (clamshell), 8 (non-clamshell)
Maximum total capacity	• 6GB (1×16 Gb devices in non-clamshell mode per subsystem) • 12GB (2×16 Gb devices in clamshell mode per subsystem)	• 16GB (1×16 Gb devices in non-clamshell mode per subsystem) • 32GB (2×16 Gb devices in clamshell mode per subsystem)
Number of channels per GDDR subsystem	2	2
Maximum number of channels total per FPGA	6	16
Width per channel (bits)	16	16
Maximum per-pin data rate supported by FPGA	16 Gbps	16 Gbps
Maximum total bandwidth (No_of_channels_per_FPGA × width_per_channel × rate)	1536 Gbps	4.0 Tbps
Capacity per memory chip	8 Gb–16 Gb	8 Gb–16 Gb
Total memory per FPGA	• Up to 6 GB for non-clamshell mode • Up to 12 GB for clamshell mode	• Up to 16 GB for non-clamshell mode • Up to 32 GB for clamshell mode
Memory data rate	16 Gbps	16 Gbps

DDR

Speedster7t FPGAs include DDR4/5 interfaces ensuring that memory capacity requirements can be satisfied across a vast application space. The DDR4/5 PHY and controller in Speedster7t FPGAs are compliant to the DDR4/5 JEDEC specification. DDR4 in the Speedster7t FPGAs can operate up to 3,200 Mbps in ×4, ×8 and ×16 width configurations. The implementation supports component memories, UDIMM/SODIMM form factors as well as RDIMMs and LRDIMMs. DDR4/5 in the Speedster7t AC7t700/AC7t800 FPGAs support up to 5600 Mbps in ×4 and ×8 modes

implemented using component DRAMs, UDIMM and RDIMM. Refer to the following tables for a summary of the key specifications and features.

DDR4

All Speedster7t FPGAs allow for multi-rank support in the DDR4 interface, up to four ranks in standard mode.

The DDR4 PHY/controller can connect to the other interface subsystems or the FPGA fabric via an AXI interface with support for full, half and quarter-rate clocking. The two connectivity options include:

- A 256-bit AXI interface to the 2D NoC, which can run up to 800 MHz, and connects to interface subsystems and the FPGA fabric.
- A 512-bit AXI direct-to-fabric interface, which can run up to 400 MHz (not available for AC7t700/AC7t800)

Speedster7t FPGAs support AXI compliant low-power interfacing. The DDR4 PHY/controller provides three options for low-power mode:

- A 256-bit AXI interface in low power
- A 512-bit AXI interface in low power (not available for AC7t700/AC7t800)
- Memory controller core logic in low power

The option also exists to bypass the entire DDR4 PHY and use these I/O for driving low-performance interfaces such as I^2C, or for optics control, LEDs, etc.

Table 12 • DDR4 Key Specifications and Features on Speedster7t FPGAs

DDR4 Feature		Support in Speedster7t FPGAs
Memory types		Component, UDIMM, SO-DIMM, RDIMM, LRDIMM (†)
Memory configurations		×4, ×8, ×16
Maximum data rate		3200 Mbps
Burst modes		BL8, burst chop
Data path widths	Non-ECC	16-bit, 32-bit, 64-bit
	ECC	32-bit + 7-bit ECC, 64-bit + 8-bit ECC
Multi-rank support		4 (standard)
AXI interface		AXI4 with read reorder buffer and port data widths of 256 and 512 bits

DDR4 Feature	Support in Speedster7t FPGAs

Table Note

† AC7t700/AC7t800 only supports UDIMM

DDR5

Speedster7t AC7t700/AC7t800 FPGAs support DDR5 memory, in addition to DDR4. The Speedster7t AC7t700/AC7t800 FPGAs can also be used in DDR4 mode, when only one of the channels is utilized, making the solution similar to the Speedster7t AC7t1400/AC7t1500 FPGAs, and as detailed above.

Optionally, the entire DDR5 PHY may be bypassed and the I/O used for driving low-performance interfaces.

Table 13 • DDR5 Key Specifications and Features on Speedster7t AC7t700/AC7t800 FPGAs

DDR5 Feature		Support in Speedster7t AC7t700/ AC7t800 FPGAs
Memory types		Component
Memory configurations		×4, ×8, ×16
Maximum data rate		5600 Mbps
Burst modes		BL8, burst chop
Data path widths	Non-ECC	8-bit, 16-bit, 32-bit, 64-bit
	ECC	64-bit + 16-bit ECC
Multi-rank support		4
AXI interface		AXI4 with read reorder buffer and port data widths of 256

Chapter 7 : Speedster7t FPGA Configuration

For normal operation, the Speedster7t FPGA core requires configuration by the end user. Speedster7t FPGAs can be configured via one of four interfaces:

- Flash
- JTAG
- CPU Mode
- PCI Express (PCIe)

A configuration bitstream is generated in ACE by selecting the appropriate configuration interface. The configuration mode of the FPGA is controlled via mode select pins on the configuration interface of the FPGA. These pins can be driven via hardware on the board or by another device such as a CPLD. The option exists to generate an encrypted and authenticated bitstream. If this feature is used, the Speedster7t FPGA first secures the hardware and then authenticates and decrypts the bitstream before programming the FPGA fabric.

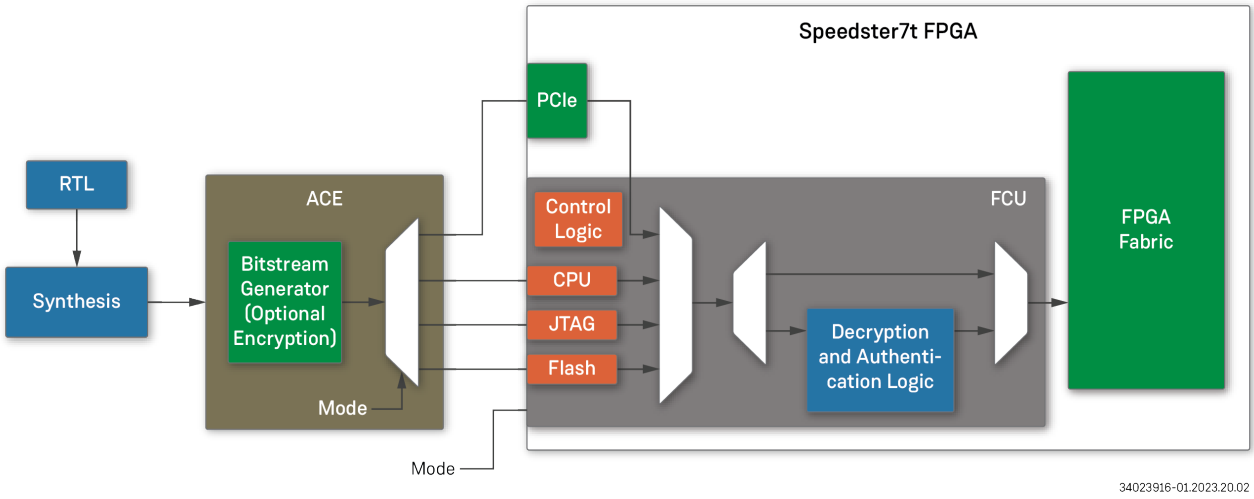


Figure 12 • Bitstream Generation and Configuration Process

Flash Mode

The serial flash programming mode allows flash memories to be used to configure the Speedster7t FPGA. In this mode, the Speedster7t FPGA is the controller and supplies the clock. Flash programming supports SPI (single-bit interface to the flash memory), dual (two-bit interface to the flash memory), quad (four-bit interface to the flash memory) and octa (eight-bit interface to the flash memory) modes. Additionally, the Speedster7t FPGA can interface to one device (1D) or four devices (4D) of flash memory modules on the board. The bitstream size is entirely dependent on the size of the fabric. It is important that the flash solution chosen is large enough to store the bitstream data.

Flash mode also supports the remote update with fallback option feature, wherein two bitstreams can be simultaneously stored in the flash device and either one chosen to program the FPGA. The update can be triggered remotely via a user application that writes to appropriate registers on the Speedster7t device. If bitstream programming fails for some reason, the fallback logic loads a known good bitstream which allows the device to resume normal operation.

JTAG Mode

The Speedster7t FPGA JTAG Tap controller is IEEE Std 1149.1 and 1149.6 (AC JTAG) compliant. The JTAG interface also provides debug capability for the Achronix on-chip logic analyzer tool, Snapshot, and other debug tools. The Speedster7t FPGA can be configured as a single JTAG device, or as part of a series of devices within a system connected on the JTAG chain.

CPU Mode

In CPU mode, an external device acts as the controller for programming operations. This mode offers a high-speed method for loading configuration data. CPU mode uses either a 1-, 8-, 16-, or 32-bit wide parallel interface. This mode provides for the widest data interface and a maximum supported clock rate of 250 MHz.

> **Note**
> If interested in using 128-bit mode, please contact Achronix for support.

PCIe Mode

PCIe mode requires two-stage programming. First, the clocks and PCIe subsystem are configured via flash, JTAG, or CPU. When the PCIe interface is enabled, the remainder of the bitstream is loaded via PCI Express.

Bitstream Security Features

Achronix recognizes the importance of protecting the sensitive IP placed onto the FPGA. To provide a high level of protection, Speedster7t FPGAs have a number of features to support bitstream encryption as well as authentication. These features ensure that the design configuration on the FPGA cannot be accessed and also ensures that the design is the one intended. Speedster7t FPGAs provide this high level of security through the following features:

- Support for ECDSA authenticated and AES-GCM encrypted bitstream
- Dynamic power analysis (DPA) protection to prevent side-channel attacks
- Physically unclonable function (PUF) for tamper-proof protection
- Securely stores both public and encrypted private keys

With this security solution deployed, customer designs are secure. Even with possession of the device, the underlying design cannot be extracted, cannot be reverse engineered, nor can the design be altered in any way.

Chapter 8 : Speedster7t FPGA Debug

Snapshot

Snapshot is the real-time design debugging tool for Achronix FPGAs and eFPGA cores. The Snapshot debugger, which is embedded in ACE software, delivers a practical platform to observe the signals of a user design in real-time. To use the Snapshot debugger, the Snapshot macro must be instantiated inside the user RTL. After instantiating the macro and programming the FPGA, the design may be observed through the Snapshot debugger GUI within ACE, or via the `run_snapshot` Tcl command API.

The Snapshot macro can be connected to any logic signal mapped to the Achronix core, to monitor and potentially trigger on that signal. Monitored signal data is collected in real time in regular BRAMs prior to being transferred to the ACE Snapshot GUI. The Snapshot macro has configurable monitor width and depth, as well as other configuration parameters, allowing control over resource usage.

The ACE Snapshot GUI interacts with the hardware via the JTAG interface. Interactively-specified trigger conditions are transferred to the design, and collected monitor data is transferred back to the GUI, which displays the data using a built-in waveform viewer. The following figure shows the components involved in a Snapshot debug session:

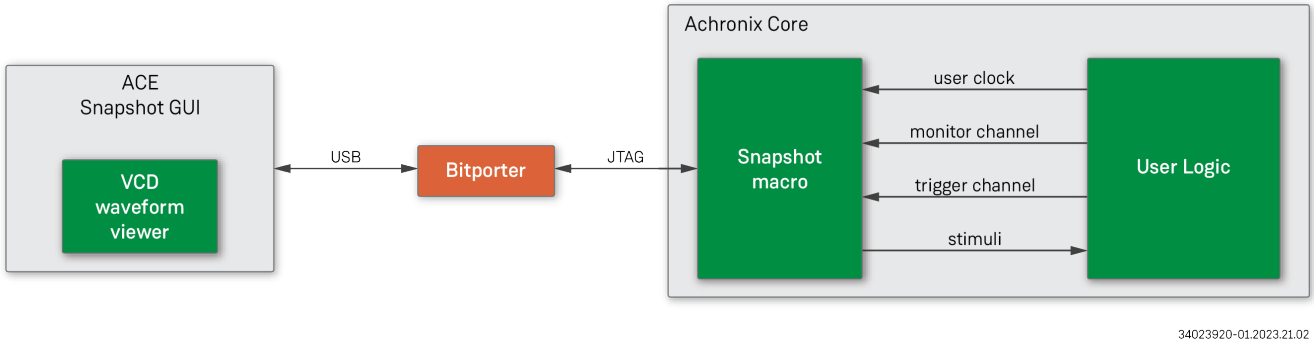


Figure 13 • Snapshot Overview

Features

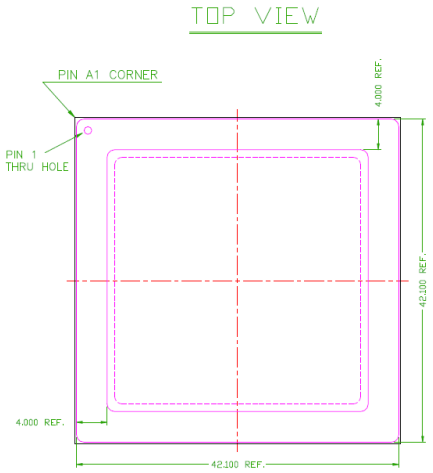
The Snapshot macro samples user signals in real time, storing the captured data in one or more BRAMs. The captured data is then communicated through the JTAG interface to the ACE Snapshot GUI. The implementation supports the following features:

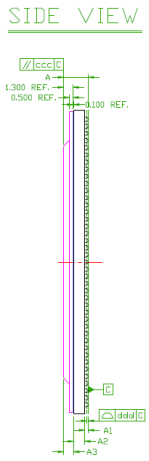
- Monitor channel capture width of 1 to 4064 bits of data.
- Monitor channel capture depth of 512 to 16384 samples of data at the user clock frequency.
- Trigger channel width of 1 to 40 bits.
- Supports up to three separate sequential trigger conditions. Each trigger condition allows for the selection of a subset of the trigger channel, with AND or OR functionality.

- Bit-wise support for edge-sensitive (rise/fall) or level-sensitive triggers.
- The ACE Snapshot GUI allows the specification of trigger conditions and circuit stimuli at runtime.
- An optional initial trigger condition, specified in RTL parameters, to allow capture of data immediately after startup, before interaction with the ACE Snapshot GUI.
- A stimuli interface, 0 to 512 bits wide, that allows the driving values into the Achronix core logic from Snapshot. Stimuli values are specified with the ACE Snapshot GUI and made available before data capture.
- Optionally, the data capture can include values prior to the trigger event. This pre-store amount can be specified in increments of 25% of the depth.
- Captured data is saved in a standard VCD waveform file. The ACE Snapshot GUI includes a waveform viewer for immediate feedback.
- The VCD waveform file includes a timestamp for when the Snapshot was taken.
- ACE automatically extracts the names of the monitored signals from the netlist, for easy interpretation of the waveform.
- A repetitive trigger mode, in which repeated Snapshots are taken and collected in the same VCD file.
- The JTAG interface can be shared with the user design.
- A Tcl batch/script mode interface is provided via the `run_snapshot` Tcl command.

Chapter 9 : Speedster7t Packaging Information

AC7t700/AC7t800 1677-Pin FBGA





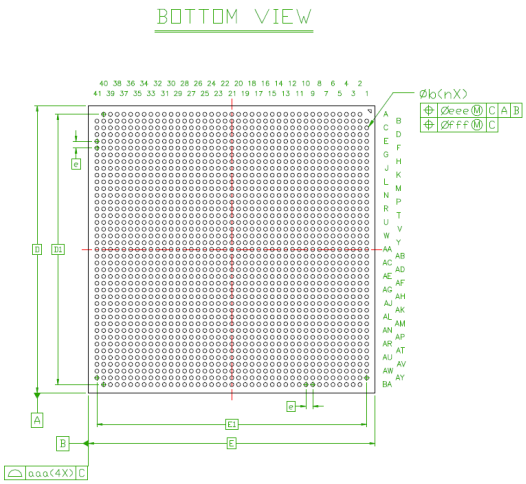


Figure 14 • 1677-Pin FBGA Package

AC7t1400/AC7t1500 2597-Pin FBGA

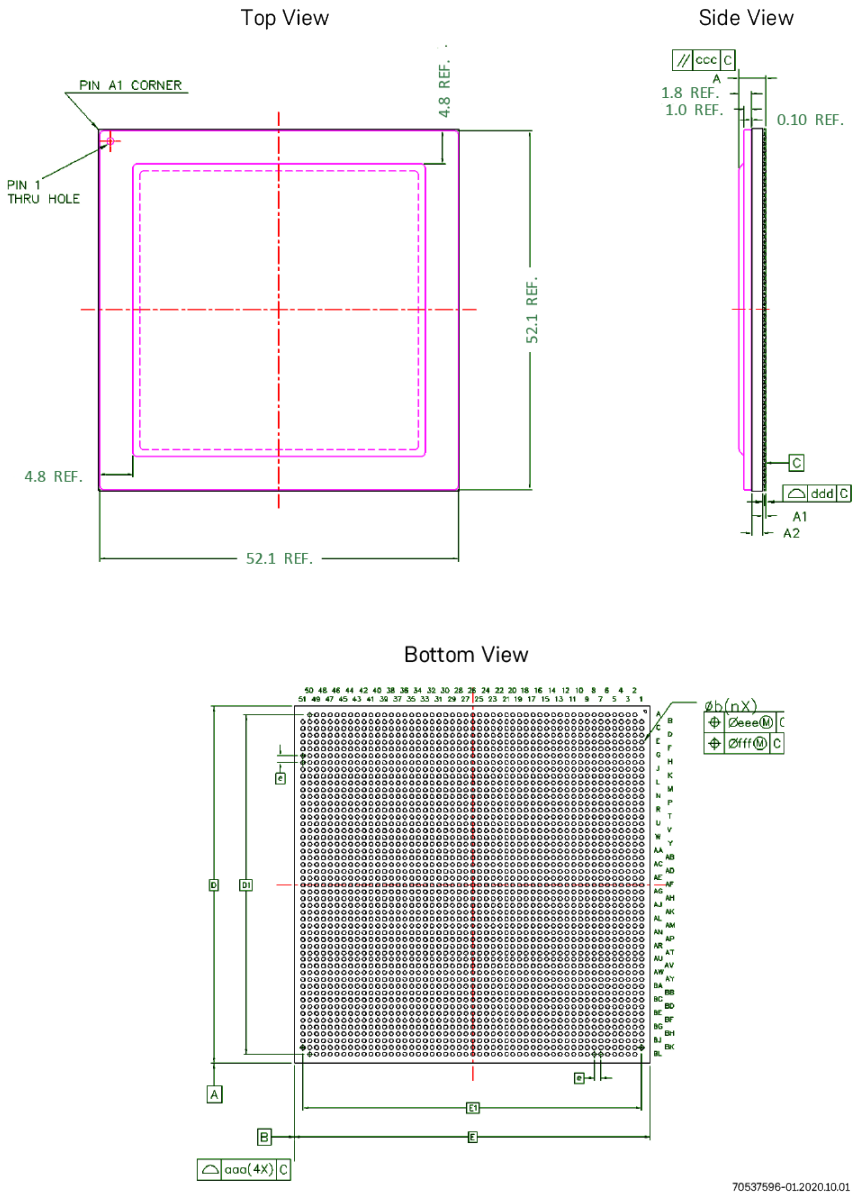


Figure 15 • 2597-Pin FBGA Package

Table 14 • FBGA Package Dimensions Details

Parameter	Symbol	AC7t1400/AC7t1500			AC7t700/AC7t800		
		Min	Nom	Max	Min	Nom	Max
TOTAL THICKNESS (mm)	A	3.757	3.952	4.147	3.257	3.452	3.647
STAND OFF (mm)	A1	0.400	–	0.600	0.400	–	0.600
SUBSTRATE THICKNESS (mm)	A2		1.552			1.552	
BODY SIZE	E	52.5 BSC			42.5 BSC		
	D						
BALL DIAMETER (mm)		0.600					
BALL WIDTH (mm)	b	0.500	–	0.700	0.500	–	0.700
BALL PITCH (mm)	e	1.00 BSC					
BALL COUNT	n	2597			1677		
EDGE BALL CENTER TO CENTER (mm)	E1	49.94 BSC			40 BSC		
	D1						
PACKAGE EDGE TOLERANCE (mm)	aaa	0.200					
TOP PARALLELISM (mm)	CCC	0.350					
CO PLANARITY (mm)	ddd	0.200					
BALL OFFSET (PACKAGE) (mm)	eee	0.250					
BALL OFFSET (BALL) (mm)	fff	0.100					

Chapter 10 : Speedster7t I/O Electrical Specification

This section provides a brief summary of the target electrical specification of the MSIO and REFIO. The MSIO can be found in the GPIO as well as MSIO portions of the CLKIO interface. The REFIO signals are only a part of the CLKIO. The relevant electrical specifications from the associated standards document are used for compliance testing.

Absolute Maximum Ratings

The following table lists absolute maximum ratings, beyond which damage to the device may occur.

Table 15 • Absolute Maximum Ratings

Parameter Symbol	Min	Typ	Max	Unit	Description
V_{DDIO}	1.07	1.1	1.14	V	Analog supply for CLKIO (CLKIO_*_V_{DDIO}) and GPIO (GPIO_*_V_{DDIO}): • CLKIO bank voltages: 1.8V, 1.5V • GPIO bank voltages: 1.8V, 1.5V, 1.35V, 1.2V, 1.1V
	1.16	1.2	1.24	V	
	1.31	1.35	1.4	V	
	1.45	1.5	1.55	V	
	1.75	1.8	1.86	V	
V_{REF}	0.53	0.55	0.57	V	Reference voltage supply for CLKIO (CLKIO_*_V_{REF}) and GPIO (GPIO_*_V_{REF}) .
	0.58	0.6	0.62	V	
	0.65	0.675	0.7	V	
	0.73	0.75	0.78	V	
	0.87	0.9	0.93	V	
T_J	-40	25	105	°C	Junction operating temperature.

GPIO Electrical Specification

The following table lists the target electrical specification for all GPIO in Speedster7t FPGAs.

Table 16 • GPIO Electrical Specification

Parameter Symbol	Min	Typ	Max	Unit	Description
C_{IN}			5	pF	Input capacitance.
I_L			30	uA	Input/Output leakage.
I_{L_VREF}			5	uA	V_{REF} pad leakage.
I_{PU}	30		150	uA	Pad pull-up (when enabled), V_{in} = 0 V.
I_{PD}	30		150	uA	Pad pull-down (when enabled), V_{in} = V_{DDIO}.
ODT_{CAL}	-10%		10%		Calibrated ODT accuracy (MSIO_ZCAL in same bank).
ODT_{CAL_DIFF}	-20%		20%		Calibrated differential ODT accuracy (MSIO_ZCAL in same bank).
V_{INL}	-200		V_{REF}-90	mV	Input logic low level.
V_{INH}	V_{REF}+90		V_{DDIO}+200	mV	Input logic high level.
F_{MAX}			500	MHz	Maximum I/O frequency (Dependent on-board level loading and SI).
I_{DRV}	2		16	mA	1.8V LVCMOS drive levels.
V_{ST}	30	40	60	mV	Schmitt trigger hysteresis.
V_{REF}	0.3*V_{DDIO}		0.7*V_{DDIO}	V	Supported V_{REF} levels.
SR_{HSUL}	2			V/ns	Slew rate for HSUL configuration with C_{load} = 5 pF, R_{out} = 50Ω and V_{DDIO} = 1.8V.
SR_{HSTL}	0.83			V/ns	Slew rate for HSTL configuration with C_{load} = 20 pF, R_{out} = 50Ω and V_{DDIO} = 1.8V.
SR_{SSTL}	0.6			V/ns	Slew rate for SSTL configuration with C_{load} = 30 pF, R_{out} = 50Ω and V_{DDIO} = 1.8V
SR_{LVCMOS}	3			V/ns	Slew rate for LVCMOS configuration with C_{load} = 5 pF and V_{DDIO} = 1.8V.

CLKIO Electrical Specification

The following table lists the target electrical specification for all CLKIO in Speedster7t FPGAs.

Table 17 • CLKIO Electrical Specification

Parameter Symbol	Min	Typ	Max	Unit	Description
C_{IN}			5	pF	Input capacitance.
I_L			30	uA	Input/Output leakage.
ODT_{CAL_DIFF}	-15%		15%		Calibrated differential ODT accuracy (MSIO_ZCAL in same bank).
$V_{IN\_DIFF\_PEAK}$	100	350	800	mV	Input levels in differential RX mode.
V_{CM_DC}	0.3	1.2	1.425	V	Board level DC coupling receive common mode.
V_{CM_AC}	0.6		1.1	V	Board level AC coupling receive common mode.
$Jitter_{intrinsic}$			0.3	ps rms 12 kHz-75 MHz	Intrinsic receive buffer jitter for 150 MHz reference clock with 200 mV differential peak swing and 400 ps rise/fall time (slew rate of 1V/ns).
F_{MAX}			1000	MHz	Maximum I/O frequency (dependent on-board level loading and SI).
I_{DRV}	2		16	mA	1.8V LVCMOS drive levels.

Chapter 11 : Speedster7t FPGA Power Rails, Part Numbers and Ordering Information

Power Supplies

Table 18 • Speedster7t Power Supply Requirements by Pin Name

Power Rail	Min Voltage (V)	Typ Voltage (V)	Max Voltage (V)	AC Ripple (mV pk-pk)	Description
VCC	0.84	0.85	0.86	17	Digital supply for the interface IP and I/O ring.
TS_VDDA	1.78	1.8	1.82	36	Analog power supply to the temperature sensor.
CLKIO_<NE/NW/SE/SW>_VDDIO	1.46	1.5	1.61	30	Analog supply for clock I/O.
	1.75	1.8	1.93	30	
CLKIO_<NE/NW/SE/SW>_VREF	0.73	0.75	0.8	15	Reference voltage supply for the CLKIO.
	0.87	0.9	0.96	15	
CORE_VDD (Speed grade 1 – 0.90v)	0.89	0.90	0.91	36	
CORE_VDD (Speed grade 2 – 0.85v/0.9v)	0.84	0.85 or 0.9	0.91	34	
DDR4_S0_VAA	1.78	1.8	1.82	36	Analog power supply for the DDR PLL.
DDR4_S0_VDDQ (AC7t1500/AC7t1400)	1.16	1.2	1.24	38	
DDR5_VDDQ (AC7t800/AC7t700)	1.08	1.1	1.12	34	Voltage level applicable to DDR5
	1.17	1.2	1.23	36	Voltage level applicable to DDR4
ENOC_<N/NE/NW/S/SE/SW>_PLL_VDDA	1.78	1.8	1.82	36	Analog supply for the peripheral ring of the 2D NoC PLLs.
FUSE_VDD2	1.78	1.8	1.82	36	Analog supply for the eFUSE module.
FCU_VDDIO	1.78	1.8	1.82	36	Analog supply for the GPIO associated with FCU/JTAG.

Power Rail	Min Voltage (V)	Typ Voltage (V)	Max Voltage (V)	AC Ripple (mV pk-pk)	Description
GCG_<NE/NW/SE/SW>_PLL_VDDA	1.78	1.8	1.82	36	Analog supply for the clock generator PLLs.
GDDR6_<E/W>_VDDR	0.83	0.85	0.88	34	Digital supply for GDDR6 PHY. This supply is used for level shifting input signals from VDDR to VDDA domain and all output signals from VDDA to VDDR domain.
GDDR6_<E/W>_VDDA	0.83	0.85	0.87	26	Analog power supply for GDDR6 PHY. This supply is used for digital logic, custom digital, data pipes and receive delay lines.Also used as analog circuit supply, clocking, global and local clock trees.
GDDR6_<E/W>_VDDIO	1.32	1.35	1.38	27	GDDR6 I/O power supply.
GDDR6_<E/W>_VDDP	1.32	1.35	1.38	27	PLL supply for GDDR6 PHY.
SRDS_N_PA_VDDH	1.16	1.2	1.3	10	SerDes analog high-power supply.
SRDS_N_PA_VDDL	0.73	0.75	0.81	10	SerDes analog low-power supply.
GPIO_<N0/S0>_VDDIO	1.07	1.1	1.14	30	Analog supply for the GPIO.
	1.16	1.2	1.24	40	
	1.31	1.35	1.4	50	
	1.45	1.5	1.55	60	
	1.75	1.8	1.86	100	
GPIO_<N0/S0>_VREF	0.53	0.55	0.57	15	Reference voltage supply for the GPIO.
	0.58	0.6	0.62	20	
	0.65	0.675	0.7	25	
	0.73	0.75	0.78	30	
	0.87	0.9	0.93	50	

Available Part Numbers

Table 19 • Speedster7t Available Part Numbers

Device	Temp. Range	Speed Grade	IO_VCC Voltage(V)	CORE_VDD Voltage (V)	Ethernet[1] (Gbps)	SerDes[2] (Gbps)	GDDR6[2](Gbps)	PCIe[2]	DDR4[2] (Mbps)	DDR5[2] (Mbps)
AC7t1500-F53B1C1	Commercial	1	0.85	0.90	400	112	16	Gen5	3,200	-
AC7t1500-F53B1C2		2		0.85/0.9	200	56				
AC7t1500-F53B1I2	Industrial	2		0.85	200	56				
AC7t1400-F53B1C1	Commercial	1	0.85	0.90	400	112	16	Gen5	3,200	-
AC7t1400-F53B1C2		2		0.85/0.9	200	56				
AC7t1400-F53B1I2	Industrial	2		0.85	200	56				
AC7t800-F43A0C1	Commercial	1	0.85	0.90	400	112	16	Gen5	3,200	5,600
AC7t800-F43A0C2		2		0.85						
AC7t800-F43A0I2	Industrial	2		0.85						
AC7t700-F43A0C1	Commercial	1	0.85	0.90	400	112	16	Gen5	3,200	5,600
AC7t700-F43A0C2		2		0.85						
AC7t700-F43A0I2	Industrial	2		0.85						

Table Notes

1. Maximum throughput for a single Ethernet MAC (or link). The device supports multiple links and is capable of much higher aggregate Ethernet throughput.
2. Performance parameters specify highest available performance.

Temperature Ranges

Achronix Speedster7t FPGAs can support the following temperature grades (junction temperature listed):

- Extended Commercial (C): 0°C to +105°C
- Industrial (I): –40°C to +105°C

Ordering Codes

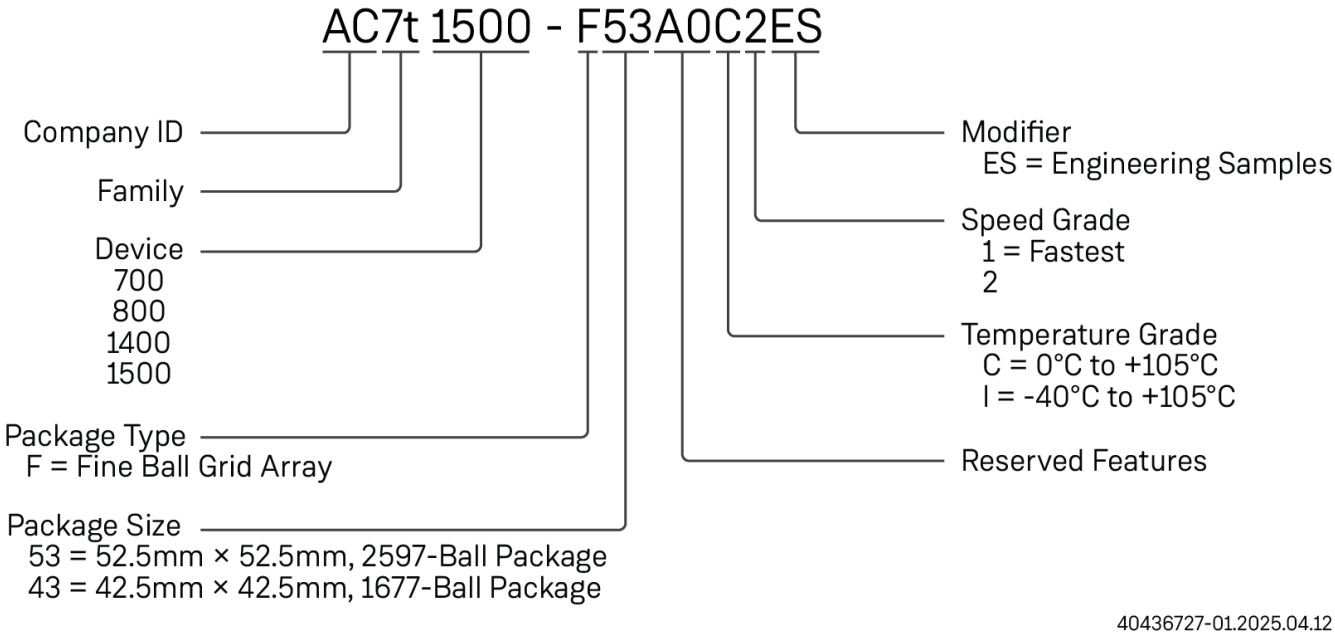


Figure 16 • Speedster7t FPGA Ordering Codes

Chapter 12 : Related Documents

Listed below are various application notes and user guides useful for the design applications targeting Speedster7t FPGAs:

> **Note**
>
> These and other documents are available for download on our website: www.achronix.com/support/docs[3]

Application Notes

Document Title	Description
Migrating to Achronix FPGA Technology (AN023)[4]	Many users transitioning to Achronix FPGA technology are familiar with existing FPGA solutions from other vendors. Although Achronix technology and tools are similar to existing FPGA technology and tools, there are some differences. Understanding these differences is necessary to achieving the very best performance and quality of results (QoR).
PCIe Enumeration of Speedster7t FPGAs (AN027)[5]	This Application Note provides the steps to attain enumeration from a non-enumerated device with a PCIe interface and from an already enumerated device.

3 https://www.achronix.com/support/docs
4 https://www.achronix.com/documentation/migrating-achronix-fpga-technology-an023
5 https://www.achronix.com/documentation/pcie-enumeration-speedster7t-fpgas-an027

User Guides

General Guides

Document Title	Description
ACE Installation and Licensing Guide (UG002)[6]	This guide covers software installation and licensing of ACE software under both Windows and Linux operating software. **Note** As of ACE release 10.3, Achronix will no longer publish ACE GUI help in the form of a PDF user guide. The contents are accessible via the built-in ACE help system.
ACE User Guide (UG070)[7]	This guide is a reference manual for ACE, used for placing, routing, configuring, and debugging Speedcore eFPGAs and Speedster FPGAs. ACE works in conjunction with third-party synthesis and simulation tools to provide a complete design environment for Achronix FPGAs.
Design Flow User Guide (UG106)[8]	This user guide covers various aspects of the Achronix toolchain design flow.
Getting Started User Guide (UG105)[9]	This guide serves as a concise introduction to the Achronix tool flow using the quickstart design included with all ACE installations.
Simulation User Guide (UG072)[10]	The Achronix tool suite includes synthesis and place-and-route software that maps RTL designs (VHDL or Verilog) into Achronix devices. In addition to synthesis and place-and-route functions, the Achronix software tools flow also supports simulation at several flow steps (RTL, Synthesized Netlist, and Post Place-And-Routed Netlist). This guide covers the simulation flow for Achronix devices.
Snapshot User Guide (UG016)[11]	Snapshot is the real-time design debugging tool for Achronix FPGAs and cores. This guide details the setup and operation of the Snapshot feature using a simple reference design.

6 https://www.achronix.com/documentation/ace-installation-and-licensing-guide-ug002
7 https://www.achronix.com/documentation/ace-user-guide-ug070
8 https://www.achronix.com/documentation/design-flow-user-guide-ug106
9 https://www.achronix.com/documentation/getting-started-user-guide-ug105
10 https://www.achronix.com/documentation/simulation-user-guide-ug072
11 https://www.achronix.com/documentation/snapshot-user-guide-ug016

Document Title	Description
Synthesis User Guide (UG018)[12]	This user guide describes how to use Synplify Pro from Synopsys to synthesize a design and generate a netlist for implementation in Achronix devices. Suggested optimization techniques are also included.

Hardware Design User Guides

Document Title	Description
Software Development Kit User Guide (UG107)[13]	This Guide introduces the Achronix Software Development Kit and details each of the provided structures and functions.
Speedster7t 2D Network on Chip User Guide (UG089)[14]	The Speedster7t FPGA family of devices has a network hierarchy that enables extremely high-speed dataflow between the FPGA core and the interfaces around the periphery, as well as between logic within the FPGA itself. This on-chip network hierarchy supports a cross-sectional bidirectional bandwidth of 20 Tbps. It supports a multitude of interface protocols including GDDR6, DDR4/5, 400G Ethernet, and PCI Express Gen5 data streams, while greatly simplifying access to memory and high-speed protocols. Achronix's two-dimensional network on chip (2D NoC) provides for read/write transactions throughout the device, as well as specialized support for 400G Ethernet streams in selected columns. The features of the 2D NoC described in this user guide generally pertain to the entire Speedster7t family of devices. In order to help users understand specific connections and features of the 2D NoC, this user guide focuses on the 2D NoC as implemented in the AC7t1500 device.
Speedster7t Board Design Guide (UG101)[15]	The Speedster7t FPGAs includes several advanced interfaces that require careful design in order to operate at their peak performance. This guide is intended as a general overview of PCB design principles that help the designer get the most out of the Speedster7t FPGA. This guide is broken down by system components: the Ethernet, PCIe5, GDDR6 memory and DDR4 memory interfaces.
Speedster7t Clock and Reset Architecture User Guide (UG083)[16]	This document explains the architecture of the different clock networks in a Speedster7t FPGA and and provides information on how to use the clocks.

12 https://www.achronix.com/documentation/synthesis-user-guide-ug018
13 https://www.achronix.com/documentation/software-development-kit-user-guide-ug107
14 https://www.achronix.com/documentation/speedster7t-2d-network-chip-user-guide-ug089
15 https://www.achronix.com/documentation/speedster7t-board-design-guide-ug101
16 https://www.achronix.com/documentation/speedster7t-clock-and-reset-architecture-user-guide-ug083

Document Title	Description
Speedster7t Component Library User Guide (UG086)[17]	The Achronix Speedster7t component library provides the user with building blocks that may be instantiated into the user's design. These components provide access to low-level fabric primitives, complex I/O blocks, and higher level design components. Each library element entry describes the operation of the component as well as any parameters that must be initialized. Verilog and VHDL templates are also provided to aide in the implementation of the user's design.
Speedster7t Configuration User Guide (UG094)[18]	At startup, Speedster7t FPGAs require configuration via a bitstream. This user guide details the programming process through one of four available interfaces in the FPGA configuration unit (FCU), the logic controlling the configuration process.
Speedster7t DDR User Guide (UG096)[19]	The Achronix Speedster7t FPGA family provides DDR subsystems that enable the user to fully utilize the low latency and high-bandwidth efficiency of these interfaces for critical applications such as high-performance compute and machine learning systems.
Speedster7t Ethernet User Guide (UG097)[20]	Speedster7t devices include high-speed Ethernet interfaces, which can support a wide variety of Ethernet packet protocols and speeds of up to 400 Gbps per channel. These Ethernet interfaces are paired with latest generation SerDes which individually support 100 Gbps data rates. With eight of these SerDes per Ethernet interface, each interface can support 2× 400 Gbps Ethernet IP channels.
Speedster7t GDDR6 User Guide (UG091)[21]	The Speedster7t FPGA family provides multiple GDDR6 subsystems enabling full utilization of the high-bandwidth efficiency of these interfaces. This guide provides the details for implementing the GDDR6 IP in custom designs.
Speedster7t GPIO User Guide (UG112)[22]	This document describes the Speedster7t FPGA GPIO pins, their various features, how to configure them, any design considerations to be taken into account, and the tools required to implement them.

17 https://www.achronix.com/documentation/speedster7t-component-library-user-guide-ug086
18 https://www.achronix.com/documentation/speedster7t-configuration-user-guide-ug094
19 https://www.achronix.com/documentation/speedster7t-ddr-user-guide-ug096
20 https://www.achronix.com/documentation/speedster7t-ethernet-user-guide-ug097
21 https://www.achronix.com/documentation/speedster7t-gddr6-user-guide-ug091
22 https://www.achronix.com/documentation/speedster7t-gpio-user-guide-ug112

Document Title	Description
Speedster7t Machine Learning Processor User Guide (UG088)[23]	The machine learning processor block (MLP) is an array of up to 32 multipliers, followed by an adder tree, an accumulator, and a rounding/ saturation/normalize block.The MLP also includes two memory blocks, a BRAM72k and LRAM2k, that can be used individually or in conjunction with the array of multipliers. The number of multipliers available varies with the bit width of each operand and the total width of input data. When the MLP is used in conjunction with a BRAM72k, the amount of data inputs to the MLP block increases along with the number of multipliers available.
Speedster7t Pin Connectivity User Guide (UG084)[24]	This user guide lists each of the I/O pin groups available in the Speedster7t 7t1500, 7t1400, and 7t800 devices, their functionality and recommended connection guidelines.
Speedster7t Power Estimator User Guide (UG093)[25]	The Achronix Speedster7t Power Estimator tool provides a platform to calculate the power requirements for the Achronix 7nm standalone FPGAs. This user guide gives a detailed overview of the thermal and power needs depending on the device, environment and utilization of components in the design.
Speedster7t Power and Sequencing User Guide (UG087)[26]	This document describes the different power supplies that are required for the Speedster7t devices and voltage tolerance levels for each of them. Also included are the connection guidelines for each of the power rails and recommendations for the power supply network sharing schemes at the board level. In addition, applicable power sequencing requirements are detailed.
Speedster7t SerDes User Guide (UG099)[27]	This product guide describes the function and operation of the Achronix Speedster7t family FPGA (AC7t1500/AC7t1400 and AC7t800) SerDes for multi-standard applications and custom configurations.
Speedster7t Soft IP User Guide (UG103)[28]	This document describes the available soft IP cores and the methods for configuration and instantiation of each.

23 https://www.achronix.com/documentation/speedster7t-machine-learning-processor-user-guide-ug088
24 https://www.achronix.com/documentation/speedster7t-pin-connectivity-user-guide-ug084
25 https://www.achronix.com/documentation/speedster7t-power-estimator-user-guide-ug093
26 https://www.achronix.com/documentation/speedster7t-power-and-sequencing-user-guide-ug087
27 https://www.achronix.com/documentation/speedster7t-serdes-user-guide-ug099
28 https://www.achronix.com/documentation/speedster7t-soft-ip-user-guide-ug103

Chapter 13 : Speedster7t FPGA Datasheet Revision History

Revision History

Version	Date	Description
1.0	24 Mar 2020	• Initial Achronix release.
1.1	12 Jun 2020	• Updated number of special-purpose I/O (SPIO) in table, **Speedster7t FPGA Family Features Table** (page 3). • Added new sections: ◦ **Special-Purpose I/O (SPIO)** (page 19) ◦ Speedster7t FPGA Timing Data
1.2	07 Aug 2020	• Added new sections for Fabric and Macro in the chapter, Speedster7t FPGA Timing Data.
1.3	02 Oct 2020	• Added the chapter, **Speedster7t Packaging Information** (page 37) with details on the 2597-pin FBGA.
1.4	18 Mar 2021	• Added support for the Speedster7t AC7t1550 FPGA. • Added the chapter, Speedster7t FPGA Cryptographic Engine.
1.5	29 Jun 2021	• Updated Speedster7t Product Family table, and ordering codes. • Replaced all instances of "NoC" replaced with "2D NoC" and made minor edits.
1.6	21 Jan 2022	• Corrected maximum number of memory chips for GDDR6 in the chapter **Speedster7t FPGA Interface Subsystems** (page 27). • Minor clarifications and updates.
1.7	26 Jul 2022	• Corrected maximum total memory capacity for GDDR6 memory in clamshell mode in the chapter **Speedster7t FPGA Interface Subsystems** (page 27). • Added section **Speedster7t I/O Electrical Specification** (page 41). • Updated with more details for Speedster7t AC7t800 FPGAs.

Version	Date	Description
1.8	17 May 2023	• Updates to Speedster7t Speed Grade table, temperature ranges, and ordering code figure in the chapter **Speedster7t FPGA Power Rails, Part Numbers and Ordering Information** (page 44). • Updates to timing data in the chapter Speedster7t FPGA Timing Data. • Updates to Speedster7t FPGA Cryptographic Engine for Speedster7t AC7t800. • Added section on Fabric Clusters in **Speedster7t Fabric Architecture** (page 6). • Updates to Speedster7t AC7t1550 resources in **Speedster7t FPGA Family Features Table** (page 3).
1.9	05 Oct 2023	• Updates to show allowable IO configurations in **Speedster7t FPGA Interface Subsystems** (page 27). • Updates to the header to add new devices to the Speedster7t I/O Electrical Specification. • Updates to the header of Speedster7t FPGA Timing Data to add new device variant. • Updates to the header of **Speedster7t Packaging Information** (page 37) to add new variant. • Updates to Speedster7t ordering code figure in the chapter **Speedster7t FPGA Power Rails, Part Numbers and Ordering Information** (page 44) to include new device variants. • Removed DDR4 bypass mode and usage as SPIO from Speedster AC7t1500 FPGA Datasheet Addendum, this has now been validated • Deprecate references to Speedster AC7t1550 device.
1.10	08 Jan 2024	• Add specifications for Speedster7t AC7t1400/AC7t1450 FPGAs.

2.0	03 Jul 2025	• Added memory suppliers to GDDR6 spec table
		• Removed AC7t1450; added AC7t700 and AC7t800 to the product table
		• Added support for AC7t700 and AC7t800 devices
		• Updates to Speedster7t ordering code figure in the chapter **Speedster7t FPGA Power Rails, Part Numbers and Ordering Information** (page 44) to include new device variants.
		• Removed the following chapters:
		  ◦ Speedster7t FPGA Cryptographic Engine
		  ◦ Speedster7t FPGA Timing Data

2.1	11 Feb 2026	• Defeatured certain DDR4 and DDR5 device type support for AC7t700/800

Version	Date	Description
2.2	08 Apr 2026	• Minor update to the table, "Speedster7t FPGA Family Overview". • Minor edit to the section, "Feature Summary" in the chapter, **Overview** (page 1)
2.3	19 May 2026	• Fixed a typo in the table notes for the table, **"Supported Ethernet Modes"** (page 27) in the chapter, "**Speedster7t FPGA Interface Subsystems** (page 27)". • Updated document titles and links in chapter, "**Speedster7t FPGA Related Documents** (page 48)".