Speedster7t SerDes User Guide (UG099)

Speedster FPGAs

Achronix
Data Acceleration

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Chapter 1 : Introduction

The Achronix 7nm Speedster®7t FPGA family (AC7t1500/AC7t1400 and AC7t800) is specifically designed to deliver extremely high performance for demanding applications including data-center workloads and networking infrastructure. The processing tasks associated with these high-performance applications, specifically those associated with artificial intelligence, machine learning (AI/ML) and high-speed networking, represent some of the most demanding processing workloads in the data center. The Achronix Speedster7t FPGA SerDes provides the foundation for high-speed, low power interconnects between Speedster7t FPGAs and external components.

This user guide describes the function and operation of the Achronix Speedster7t SerDes PHY IP for multi-standard applications. The Speedster7t FPGA family incorporates 24 to 32 instances of high-performance, low-power, multi-standard SerDes PHY, which are highly configurable and support leading NRZ and PAM4 data center standards from 1 Gbps to 56 Gbps (NRZ) in raw mode. Protocols ranging from PCI-Express Gen5 to 112 Gbps Ethernet are supported.

Chapter 2 : Overview

The Speedster7t AC7t1500/AC7t1400 incorporates 32 SerDes transmit/receive pairs, and the AC7t800 incorporates 24 SerDes transmit/receive pairs. These high-performance, low-power, multi-standard SerDes PHYs are highly configurable and support all leading NRZ and PAM4 standards from 1 Gbps to 112 Gbps (even including standards which are currently in development).

Speedster7t FPGA SerDes PHY Highlights

- Digital DSP-based SerDes architecture, performance up to 56 Gbps while consuming ~6 mW/Gbps
- Innovative analog to digital converter (ADC) and digital signal processing (DSP) architecture supports long reach channel losses with near-end crosstalk (NEXT) noise
- Power efficient for multi-lane operation
- Configurable DSP solution supports multiple power states and loop-timed applications
- Wide tuning (1–56 Gbps), low-jitter clock generation
- Independent transmit and receive lane clocking
- DSP receiver
  - Low-power, dynamic-rate, time-interleaved ADC
  - Power scales with sampling rate and with necessary signal to noise ratio (SNR)
  - Digital clock to data recovery (CDR) quickly acquires optimum sampling times for incoming signals.
  - Blind adaptive equalizer
- Low-power transmitter
  - Low-power, voltage-mode driver able to generate 56 Gbps PAM4
  - Power scales with transmit launch swings to meet necessary channel conditions
  - Reconfigurable five-tap finite impulse response (FIR) filter
- Integrated Ethernet link training and auto-negotiation

Table 1 • Supported Standards

Supported Standards	Notes
OIF Chip-Chip/Module Backplane (OIF Common Electrical Interface – CEI)	
CEI-112G-USR/SR/MR/LR-PAM4	112 Gbps VSR/MR and LR PAM4 standard
CEI-56G-USR/XSR/VSR/MR/LR-PAM4 (supports NRZ as well)	56G VSR/MR and LR PAM4 standard

Supported Standards	Notes
CEI-28G-VSR/SR/MR (19.6-28.1 Gbps), CEI-25G-LR (19.9 – 25.8 Gbps)	28G SR/MR and LR NRZ standard
CEI-25G-LR (19.9-25.8 Gbps)	25G LR NRZ standard
CEI-11G SR/MR/LR (9.95 – 11.1 Gbps)	11G SR/MR/LR NRZ standard
CEI-6G SR/LR (4.976 – 6.375 Gbps)	6G SR/LR NRZ standard
Ethernet over Electrical Cable/Chip to Chip/Module Backplane	
Ethernet Line Bit Rate (112.5 Gbps, 106.25 Gbps, 53.125 Gbps, 26.5625 Gbps, 25.78125 Gbps, 10.3125 Gbps, 3.125 Gbps, 1.25 Gbps)	
Synchronous Ethernet (ITU-T G.8262)	• PMA same as Ethernet but supports loop timing with low-jitter, low-noise clock reference according to SyncE standard • PMA can provide the SOC a recovered reference clock from any RX lane for use in SyncE applications
802.3ck(†) – 100, 200, 400 Gbps Ethernet using 100 Gbps lanes	• 4 × 100 Gbps • 2 × 100 Gbps • 1 × 100 Gbps
802.3bs – 2017, 200 GbE (200 Gbps) and 400 GbE (400 Gbps) Ethernet using 50 Gbps lanes	• 8 × 50 Gbps • 4 × 50 Gbps
802.3cd – 2018, 50, 100, and 200 Gbps Ethernet using 50 Gbps lanes	• 4 × 50 Gbps • 2 × 50 Gbps • 1 × 50 Gbps
802.3bj – 2014, 100 Gbps Ethernet using 25 Gbps lanes	4×25 Gbps
802.3ba – 2010, 40 Gbps Ethernet using 10 Gbps lanes	4×10.3125 Gbps
802.3 – 2008, 802.3ap – 2007, 1 Gbps and 10 Gbps Ethernet using 1 Gbps and 10 Gbps lanes	• 1 × 10.3125 Gbps • 1 × 3.125 Gbps • 1 × 1.25 Gbps

Supported Standards	Notes
802.3ae-2002, 10 Gbps Ethernet using 10 Gbps lanes	• 1 × 10.3125 Gbps • 1 × 9.58464 Gbps
Synchronous Ethernet (ITU-T G.8262)	Supports loop-timing applications
Optical Chip-Module	
Interlaken	3.125 to 12.5 Gbps, 25 Gbps
Computing	
• PCI Express Gen1, Gen2, Gen3, Gen4, Gen5 (2.5 Gbps, 5.0 Gbps, 8 Gbps, 16 Gbps, 32 Gbps) • Quickpath QPI / KTI / UPI	Supports both PIPE 4.x and 5.2 specification revisions
USB 3.0/3.1	
Quickpath QPI / KTI / UPI	
Compute eXpress Link (CXL) 2.0	
Cache Coherent Interconnect for Accelerators (CCIX)	
PON	
• GPON (1.25 Gbps, 2.5 Gbps, 10.0 Gbps) • E-PON (1.25 Gbps, 2.5 Gbps, 10.0 Gbps)	• Support single frequency, either continuous or burst • No mixed frequencies
Wireless	
• CPRI (24.576 Gbps, 24.330 Gbps, 19.660 Gbps, 12.165 Gbps, 10.137 Gbps, 9.830 Gbps, 6.144 Gbps, 3.072 Gbps, 2.457 Gbps, 1.228 Gbps) • JESD204A/B/C (3.125–25 Gbps)	

Table Note

† The 802.3ck only supported in AC7t800.

SerDes Placement on Speedster7t Devices

The Speedster7t FPGAs have both PCIe and Ethernet interfaces that use the SerDes PHY. All SerDes lanes can also be used independently (raw mode). The following figure shows the placement of the interface subsystems of the Speedster7t AC7t1500/AC7t1400 and AC7t800 FPGAs.

Table 2 • Available SerDes by Speedster7t Family Device

Device	Number of SerDes	Number of Quads	Subsystem
AC7t1500	32 SerDes	8 Quads	ETH_0, ETH_1 and PCIE_1
AC7t1400	32 SerDes	8 Quads	ETH_0, ETH_1 and PCIE_1
AC7t800	24 SerDes	6 Quads	ETH_1 and PCIE_1

AC7t1500/AC7t1400

Speedster7t AC7t1500/AC7t1400 has total of 32 SerDes lanes.

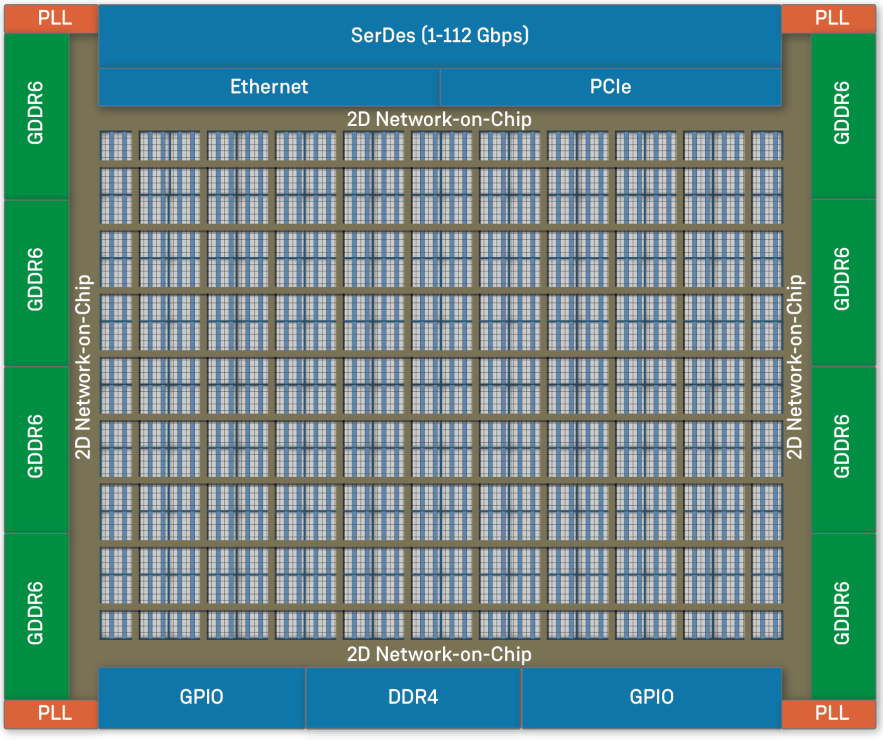

Figure 1 • Speedster7t AC7t1500/AC7t1400 SerDes Placement

The eight quads of SerDes PHY are located at the north side of the chip as shown in the following figure.

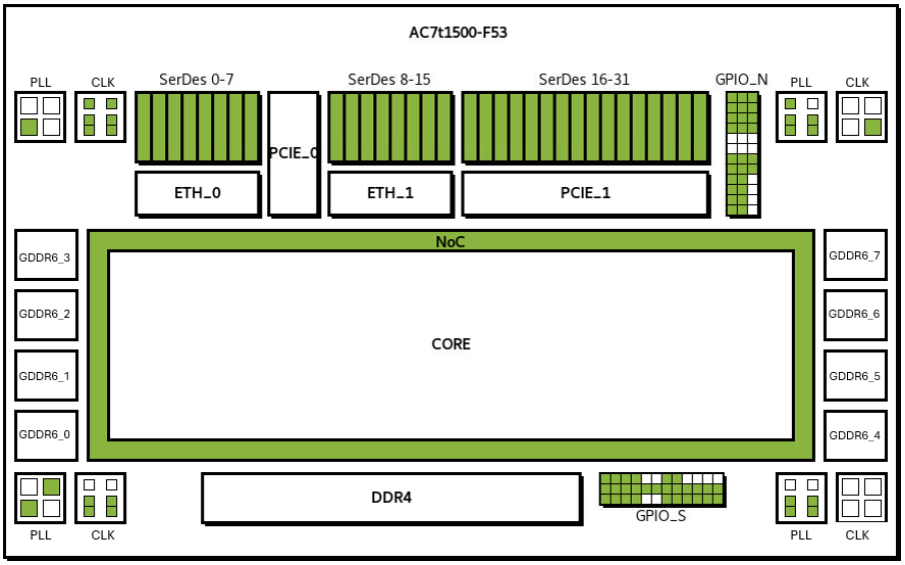

Figure 2 • Speedster7t AC7t1500/AC7t1400 FPGA Top-Level Block Diagram

Each SerDes instance is named "SerDes [x]" and they are organized as follows:

- Sixteen lanes, SerDes [31:16], are associated with a hard PCIe controller
- Eight lanes, SerDes [15:8], are associated with a hard Ethernet controller
- Eight lanes, SerDes [7:0], are associated with both the Ethernet and PCIe controllers

When operating in conjunction with the associated hard controller, the operation of the SerDes is managed by the controller per the selected protocol. All 32 SerDes lanes can be used in raw mode. A single lane is the minimum number of lanes in a quad that can be selected for raw mode.

A quad can not be split. All lanes in a quad must be associated with an Ethernet controller, PCIe controller, or raw mode. In raw mode the PCS block can be accessed directly by the user design from the FPGA fabric. The controllers are bypassed.

AC7t800

The Speedster7t AC7t800 has total of 24 SerDes lanes. The eight quads of SerDes PHY are located at the north side of the chip as shown in the following figure.

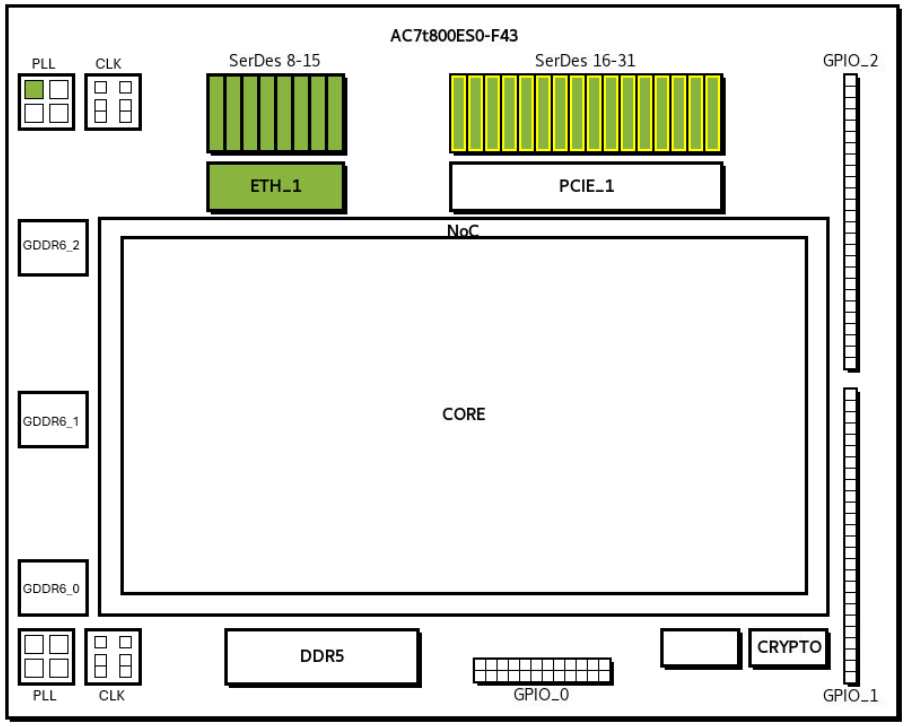

Figure 3 • Speedster7t AC7t800 FPGA Top-Level Block Diagram

For the AC7t800, each SerDes instance is named "SerDes [x]" and they are organized as follows:

- Sixteen lanes, SerDes [31:16], are associated with a hard PCIe controller
- Eight lanes, SerDes [15:8], are associated with a hard Ethernet controllers
- Eight lanes, SerDes [7:0] are not available.

> **Note**
>
> The SerDes naming convention is same as AC7t1500, so the RTL code is backward compatible, except that SerDes [7:0] are not available.

When operating in conjunction with the associated hard controller, the operation of the SerDes is managed by the controller per the selected protocol. All 24 SerDes lanes can be used in raw mode. A single lane is the minimum number of lanes in a quad that can be selected for raw mode.

A quad can not be split. All lanes in a quad must be associated with an Ethernet controller, PCIe controller, or raw mode. In raw mode the PCS block can be accessed directly by the user design from the FPGA fabric. The controllers are bypassed.

Physical Medium Attachment (PMA)

The SerDes PHYs are arranged as quads made up of four transmit/receive lanes and a common block. This common block is responsible for the following:

- Receiving the reference clock

- Generating clocks for the transmit and receive blocks (with 16-bit fractional multiplication factors and optional spread spectrum)
- Calibration
- Providing access to control/status registers

The transmit and receive portion of each lane contains an internal four-tap FIR filter. The transmitter provides a filter with output drivers that can deliver a 400–1200 mVp-p differential output voltage with adjustable slew rate.

The receive block receives the differential signal from the channel and applies equalization. It then determines level and symbol clock, captures the level and decodes per modulation into one or two bits per received symbol. The data is decoded, de-serialized, and driven out on data bus with a divided baud-clock.

The receiver supports AC and DC coupling with some restrictions on common-mode voltage. It incorporates robust automatically adjusted equalization including AGC, continuous-time linear equalizer (CTLE) with up to 20 dB gain tuned for key data rates, feed-forward equalization (FFE) and decision feedback equalizer (DFE) for robust recovery of data from impaired signals. Fast lock mode for EPON/GPON is also supported.

The SerDes includes debug features including multiple loopback modes and a non-destructive internal eye-scope in the receiver. The eye-scope can measure eye width, eye height and the bit error rate (BER).

Physical Coding Subsystem (PCS)

The Achronix PCS serves as the conduit for the SerDes data path to and from the fabric. The PCS provides several options to encode, decode, bond lanes, and reorder bits. The PCS can be bypassed if none of the features are needed for the user design.

Three types of hard PCS controllers are offered within Speedster7t FPGAs:

- A PIPE5.1-compliant mode for PCIe.
- PCS bypass mode for direct use by the fabric.
- Gearbox mode for Ethernet, supporting 66/64 bit decoding or 67/64 bit decoding.

The physical layout between the Speedster7t FPGA SerDes PHY and the PCS controllers are shown in the **previous figure** **(see figure 2)**.

ACE Support for the Speedster7t FPGA SerDes

ACE is the Achronix development tool for placing, routing, configuring, and debugging Achronix FPGAs. ACE works in conjunction with third-party synthesis and simulation tools to provide a complete design environment for Achronix FPGAs. The Speedster7t SerDes PHY can be conveniently configured and controlled through the ACE GUI.

For PCIe and Ethernet users, the ACE GUI has predefined options where the SerDes PHY can be configured easily to work seamlessly in PCIe/Ethernet mode. When the SerDes is used in raw mode, the SerDes PHY is configured via the ACE GUI. Configuration options are available by selecting the "Raw SerDes" option in the IP Library. The configuration can also be modified at runtime by writing to the control registers directly. The control and status registers are accessed through the JTAG port or by a NAP in the fabric. Refer to ***Runtime Programming of Speedster FPGAs* (AN025)**[1] for details on how to access these registers.

1 https://www.achronix.com/documentation/runtime-programming-speedster-fpgas-an025

Chapter 3 : Speedster7t SerDes Physical Medium Attachment (PMA)

Speedster7t FPGA SerDes Block Diagram

The Speedster7t SerDes PMA is composed of a common block and four transmit/receive blocks (lanes); this entire assembly is referred to as a quad, as shown in the figure below:

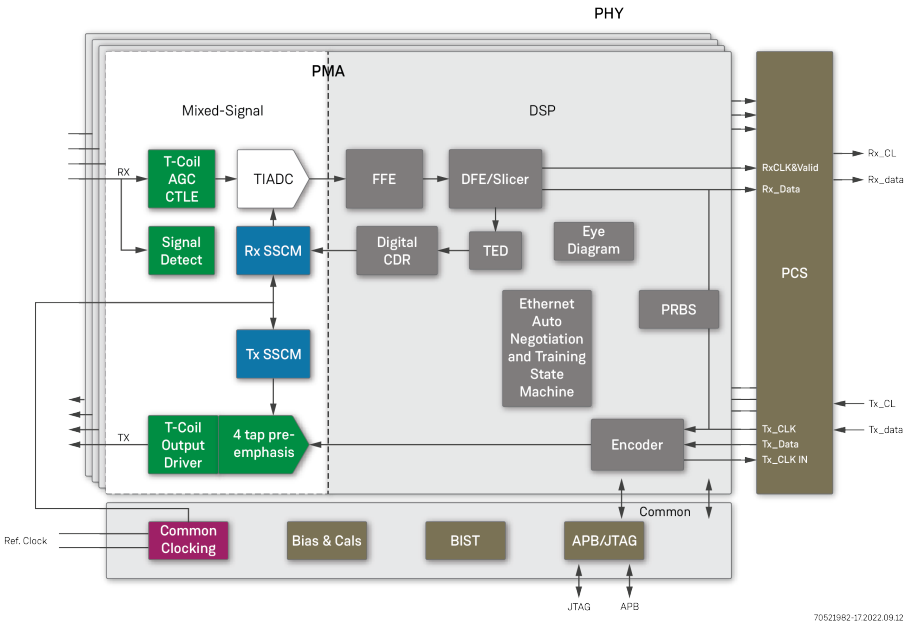

Figure 4 • Speedster7t FPGA SerDes PHY Block Diagram

Common Block

The common block performs SerDes calibration and contains control/status registers for the entire quad. The common block also receives the reference clock and generates a multiplied clock for the transmit and receive blocks (with 16-bit fractional multiplication factors and optional spread spectrum mode).

Calibration is performed automatically and can be invoked by register control. For details of the calibration control/status registers, contact Achronix Support.

The reference clock for a quad can be selectively sourced from external balls (example: SRDS_xx_REFCLK_N/P, refer to *Speedster7t Pin Connectivity User Guide* (UG084)[2] for details) or from a neighboring quad in clock share

2 https://www.achronix.com/documentation/speedster7t-pin-connectivity-user-guide-ug084

mode. The received reference clock can be selectively forwarded to neighboring quads. This option can be selected in the ACE IP configuration tool, shown in chapter, "**Speedster7t SerDes IP Software Support in ACE** (page 42)."

Clocking Architecture

The Speedster7t FPGA SerDes PHY clocking architecture provides a significant amount of configurability and flexibility. High quality clocks are generated and can be used directly by logic in the fabric.

External Reference Clocks

The Speedster7t FPGA SerDes PHY reference clocks are used by the common block LC (inductor capacitor) based PLL (LC PLL) to generate the high-speed clock, `hsrefclk`, that is distributed to the receive/transmit lane PLLs. The SerDes PHY includes the following external reference clock capabilities:

- Sourcing reference clock from the `SRDS_N[7:0]_REFCLK` external pins for AC7t1500/AC7t1400 and the SRDS_N[5:0]_REFCLK external pins for AC7t800. (Refer to ***Speedster7t Pin Connectivity User Guide*** **(UG084)**[3] `for details`)
- Sourcing reference clocks from the adjacent quad for use in the local quad (limited to quads created within a single ACXIP file).

For details refer to the "**Speedster7t PCS Block** (page 22)" chapter that shows reference clock sharing table for the SerDes reference clock mapping.

Common LC PLL

The common LC PLL contains a low quantization noise fractional synthesizer which results in a high-degree flexibility with respect to supported data rates vs. reference clock rates. This fractional synthesis capability is also leveraged to enable spread spectrum clock generation. LC PLLs provide excellent jitter characteristics for a given power.

Lane PLLs

Each transmit and receive lane has its own local PLL to enable independent operation between transmit and receive blocks as well as between different lanes. The combination of a common LC PLL and the lane PLLs provide the benefit of flexibility across standards and configurations with the performance of an LC PLL. For further details please contact Achronix Support .

Speedster7t FPGA SerDes PHY Interface

This section provides a brief description of the signal interface between the SerDes PHY and the FPGA in PCS bypass mode. These signals are on a per lane basis. "IP-Name" refers to the name of the ACXIP file and "Lane" refers to the lane number. For example: `serdes_quad_2g5_lane0_o_eth_an_link_control`.

3 https://www.achronix.com/documentation/speedster7t-pin-connectivity-user-guide-ug084

Table 3 • SerDes interface Ports

Interface Signal Name	Direction	Width	Description
IP-Name_Lane[#]_o_eth_an_done(1)	Output	1	When asserted, indicates auto-negotiation complete (link fully up, including LT and PCS).
IP-Name_Lane[#]_o_eth_an_link_control[15:0](1)	Output	16	PCS enable, one-hot encoded. When auto-negotiation (AN) is complete, one of these signals is asserted to enable the attached PCS.
IP-Name_Lane[#]_o_eth_an_link_good(1)	Output	1	When asserted, indicates AN has negotiated a link speed and is attempting to start link training/PCS.
IP-Name_Lane[#]_o_eth_an_newpage(1)	Input	1	AN newpage received indicator. A positive edge on this signal indicates a new page has been received. The FPGA should read the associated registers, write extended page information, and assert the `next_page_loaded` bit, if needed. The FPGA might also poll the equivalent register.
IP-Name_Lane[#]_i_eth_an_link_status[15:0](1)	Input	16	PCS link status. Must be asserted by the enabled PCS to indicate the link is up.
IP-Name_Lane[#]_i_tx_elecidle[3:0](1)	Input	4	Pin control of the transmit electrical idle function. For PCIe applications with synchronous electrical idle requirement: 0 – l[#] transmitter in normal operating mode. 1 – l[#] transmitter placed into electrical idle. Each bit corresponds to 16 bits of transmit data: For widths up to 20 bits, only bit 0 is active. For 32 and 40 bits, bits 1:0 are active. For 64 bits, bits 3:0 are active. For all other applications including all PM-4 rates `ictl_tx_elecidle_ln[#]` should be operated as if all were a single control (i.e., logically tie all four bits together).
IP-Name_Lane[#]_o_clk_rx_block	Output	1	Receive clock synchronous to the receive data.
IP-Name_Lane[#]_o_clk_tx_block	Output	1	Transmit clock synchronous to the transmit data.
IP-Name_Lane[#]_o_rx_data[127:0]	Output	128	Data output bus to the fabric. Software requires all 128 bits are connected to the fabric despite the receive data width chosen in the IP configuration.
IP-Name_Lane[#]_i_tx_data[127:0]	Input	128	Data input from the fabric. Software requires all 128 bits are connected to the fabric despite the transmit data width chosen in the IP configuration.
IP-Name_Lane[#]_o_rx_data_valid	Output	1	Pin output showing lock status of the receive CDR. Timed to `ck_rx_block`. 0 – CDR unlocked. 1 – CDR locked, data valid.

Interface Signal Name	Direction	Width	Description
IP-Name_Lane[#]_o_rx_signal_detect	Output	1	Unfiltered output of the analog signal detection block.

Table Notes

1. Signal not used in PCS bypass mode.

Transmit/Receive Block

The transmit and receive portion of each lane contains an internal synthesizer which allows independent rate support for each lane.

Transmit Block

The transmit block is responsible for capturing the transmit data from the fabric using a transmit clock and sending it serially off chip. This data width is variable and is dependent upon the chosen protocol standard. Within the PMA, the data is modulated (NRZ/PAM4) and serialized before being transmitted. There is an optional four-tap pre-emphasis filter to help improve the channel signal quality.

Transmit Equalization

The transmitter includes a five-tap digital FIR filter which boosts the relative amplitude of higher frequency data patterns by adjusting the amplitude of the bit/level being transmitted based on the values of preceding and succeeding bits.

In many cases, the PCIe/Ethernet subsystems attached to the SerDes properly adjust the transmit equalization during the establishment of the link. The transmit equalization can be adjusted manually to match channel requirements. The coefficient values can be overridden by writing new values to the transmit FIR coefficients in the CSR registers space.

Table 4 • Transmit Lane Features

Parameter	Design Specification
Output Driver Voltage	• Up to 1200 mVdiff-pkpk • Programmable
Transmit Coupling (1)	Supports: • External AC coupling • Floating DC coupled receive termination • DC coupling, for selected receive termination common modes.

Parameter	Design Specification
On-chip Termination	Nominal value: 90Ω
Transmit Skew	• Skew between transmit Lanes < ± 2UI • Synchronization of transmit data ensured within multiple lanes of a By-2/By-4 as well as between multiple By-1, By-2 and By-4.
Beaconing	Output enable control for beaconing.
Receiver Detection	Fully supports PCI Express receiver detection.

Table Notes

1. Contact Achronix Support for more detail; it is available under NDA.

Receiver Block

The receive channel accepts the serial differential signal from the channel and sends the data and recovered clock to the fabric. The PMA applies a continuous time linear equalization filter (CTLE) in the analog domain before the signal is digitized using a time interleaved analog-to-digital converter (TIADC). A discrete feed forward equalization filter (FFE) is used to reduce inter-symbol interference before the slicer and a decision feedback equalization (DFE) filter are used minimize decision errors. See the following table for more details.

Table 5 • Receive Lane Features

Parameter	Design Specification
Receive Input Range	Up to 1200 mVdiff-pkpk
Receive Equalization (1)	• CTLE and DSP based equalization • Blind Adaptive Receiver and Equalizer
Receive Coupling (1)	Supports: • External AC coupling • DC coupled receive termination with internal AC coupling • DC coupling without internal AC coupling for selected common modes.
Signal Detection	• Receive signal envelope detection to support Beaconing and idle-exit detection • Digital signal detection

Parameter	Design Specification
Spread spectrum	Fully supports recovery of signals with Spread Spectrum (0.5% down spread).
Frequency Accuracy	Tolerates up to -5350 ppm to +350 ppm of data frequency inaccuracy from PHY reference clock.
On-Chip Eye Monitor	Non-destructive internal eye monitoring capability.
Lock Modes	• Supports both auto-lock to incoming data when valid data is present and manual external control of lock to data • Loss-of-Lock detector functionality
Oversampling	The receive CDR supports the oversampling mode of operation.
On-chip Termination (1)	Nominal values: 90Ω.
Reference Clock source	• Independently selectable reference clock input source per lane • PMA quad includes reference clock buffers/repeaters and distribution infrastructure

Table Notes

More details can be found in Appendix I *Speedster7t FPGA SerDes Overview*, available under NDA.

Clocking

Clocking frequencies and signal geometry are specified in the following table along with a summary of features of the Common Lane.

Table 6 • Common Lane Features and Requirements

Parameter Description	Min	Typ	Max	Unit
General				
Reference clock frequency range	50		800	MHz
Frequency variation	-5350		350	ppm
Duty cycle	40	50	60	%

Parameter Description		Min	Typ	Max	Unit
Rise/fall times (20-80%)				0.2	Refclk Period
Skew between positive and negative differential inputs				10	ps
Total integrated RMS phase noise for the band of frequency ranging from 12 kHz to 20 MHz				0.7	psRMS
External Reference Clock I/O Inputs					
Input impedance	Terminated mode	40	50	60	Ω
	High-impedance mode	20k			Ω
Input Differential Voltage	PCIe	0.15			V
	LVDS	0.25		0.4	V
	LVPECL	0.525		0.95	V
Input Common Mode Voltage		0		1.2	V
Common Lane Features					
Fractional Synthesizer		• Fractional synthesizer support to eliminate integer reference clock requirements • Programmable spread spectrum generation			
Synthesizer Loop Timing		The transmit PLL supports loop timed synchronous operation.			
Synthesizer reference clock source		Independently selectable reference clock input source.			
Other clock generation (1)		• Internal heartbeat clock for power up and beaconing. • Internal clock outputs.			
Reference Clock Sources (1)		• Reference clock I/O buffer that supports a variety of input reference clock signaling (e.g., CML, LVPECL, PCIe) • On-chip CML distribution.			

Parameter Description	Min	Typ	Max	Unit

Table Notes

Request Achronix for more details which are available under NDA.

Speedster7t FPGA SerDes PMA Configuration Options

Table 7 • PMA Configurability

Parameter	Description
Number of Lanes	1 to 16, lanes must be contiguous in a single block.
PMA Rate Presets	Up to 8 line rate presets. Use for line rate change at run time.
Full Duplex Support	• Synchronized and non-synchronized full duplex operation • Independent operation of transmit and receive Lanes (power-down and reset)
Power States	Fully supports Energy Efficient Ethernet (EEE) low power states (deep sleep, fast wake). Fully supports PCIe power savings modes: • PD – Full power down on all blocks. • P2 – Lowest power/longest recovery time state. Everything powered down except Beaconing and receiver detection. • P1 – Low power/ Medium recovery time state. All P2 functionality with synthesizer powered up but transmit driver and receive paths powered down. • P0s– Some power saving / fast recovery state. All P1 functionality with receive path powered up and transmit driver powered down. • P0 – Normal full operation mode. Everything powered up.

Parameter	Description
transmit FIR [1]	Each tap is independently programmable. • C(-3) pre-cursor • C(-2) pre-cursor • C(-1) pre-cursor • C(1) post-cursor
Data Path Parallel Interface	Selectable 16/32/64/128 and 20/40 data and byte clock.

Table Notes

Request Achronix for more details which are available under NDA.

Loopback Modes

Four PHY Data loopback mode paths are available as detailed in the following diagram:

1. Internal serial transmit to receive (maximum coverage of serial path) loopback. Data is generated in and looped back to the fabric. The CTLE data bypasses the FIR and IIR filters. Referred to as NES_loopback (serial near-end-loopback). Shown as path 1
2. Internal parallel transmit to receive. Data is generated in and looped back to the fabric. Referred to as NEP_loopback (parallel near-end-loopback). Shown as path 2.
3. External serial receive to transmit. Untimed for continuity tests at low rates by external sources. Shown as path 3. It also referred to serial far-end-loopback.
4. External parallel receive to transmit. Transmits received data with respect to the device. Used to characterize the SerDes for compliance and bit error rate. Shown as path 4. It also referred to parallel far-end-loopback.

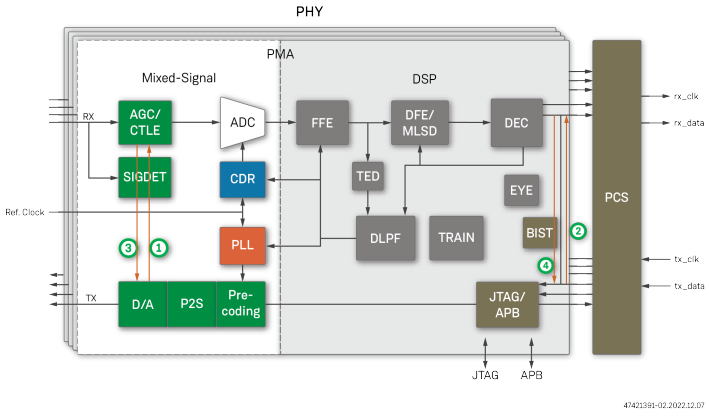

Figure 5 • Speedster7t FPGA SerDes PHY Data Loopback Modes

PMA Rate Presets

Based on the user selection of number_of_rates, there are between 1 and 8 PMA Rate Presets pages exposed, allowing customization of up to eight preset profiles.

Table 8 • Available Preset Configurations For ACE 9.2 and Beyond

Protocol Standard	SerDes Rate per Lane	PMA Electrical	PMA Width	Supported Reference Clocks	PMA Interface Frequency	PCS Data Path	Gearbox Mode
CEI-11G	11G	NRZ	64/32	156.25/312.5 MHz	171.875/343.75 MHz	PCS bypass, Gearbox Mode	66b sync, 66/67b async
CEI-12.5G	12.5G				195.3125/390.625 MHz		
CEI-25G	25G		64		390.625 MHz		
CEI-28.125G	28.125G				439.453125 MHz		
CEI-28G	28G				437.5 MHz		
CEI-50G	50G	PAM	128		390.625 MHz		
CEI-51G	51G				398.4375 MHz		
CEI-56.25G	56.25G				439.453125 MHz		
CEI-6G	6G	NRZ	40/32/20/16		150/187.5/300/375 MHz		
CPRI-10137	10.1376G		64/32		158.4/316.8 MHz		
CPRI-12165	12.16512G				190.08/380.16 MHz		
CPRI-1228	1.228G		20/16		61.4/76.75 MHz		
CPRI-19660	19.66G		64		307.1875 MHz		
CPRI-24330	24.33024G				380.16 MHz		
CPRI-2457	2.456G		40/32/20/16		61.4/76.75/122.8/153.5 MHz		
CPRI-24576	24.576G		64		384 MHz		
CPRI-3072	3.072G		40/32/20/16		76.8/96/153.6/192 MHz		
CPRI-6144	6.144G				153.6/192/307.2/384 MHz		

Protocol Standard	SerDes Rate per Lane	PMA Electrical	PMA Width	Supported Reference Clocks	PMA Interface Frequency	PCS Data Path	Gearbox Mode
CPRI-9830	9.8304G		64/32/20		153.6/307.2/491.52 MHz		
Displayport 1.62G	1.62G		40/20	156.25 MHzz	81/162 MHz		
Displayport 2.7G	2.7G				67.5/135 MHz		
Displayport 5.4G	5.4G				135/270 MHz		
Displayport 8.1G	8.1G		20		405 MHz		
Ethernet 1.25G	1.25G		20/16	156.25/312.5 MHz	62.5/78.125 MHz		
Ethernet 10.3125G	10.3125G		64/32		161.1328/322.2656 MHz		
Ethernet106.25G	106.25G	PAM4	128		415.04 MHz	PCS bypass	-
Ethernet 25.78125G	25.78125G	NRZ	64		402.8320 MHz	PCS bypass, Gearbox Mode	66b sync, 66/67b async
Ethernet 26.5625G	26.5625G				415.0391 MHz		
Ethernet 3.125G	3.125G		40/32/20/16		78.125/97.65625/156.25/195.3125 MHz		
Ethernet 53.125G	53.125G	PAM4	128		415.0391 MHz		
FC-1200	10.51875G	NRZZ	64/32		164.3555 MHz		
FC-1600	14.025G				219.53125/438.28125 MHz		
FC-3200	28.05G		64		438.28125 MHz		
FC-800	8.5G		64/32/20		132.8125/265.625/425 MHz		
FlexO-SR-28G	27.95236861G		64		436.76 MHz		
FlexO-SR-56G	55.90473722G	PAM4	128		436.76 MHz		

Protocol Standard	SerDes Rate per Lane	PMA Electrical	PMA Width	Supported Reference Clocks	PMA Interface Frequency	PCS Data Path	Gearbox Mode
High Speed Serial 112.5G	112.5G		256	156.25 MHzz	439.45 MHz	PCS bypass	-
High Speed Serial 15G	15G	NRZ	64		234.375 MHz	PCS bypass, Gearbox Mode	66b sync, 66/67b async
High Speed Serial 30G	30G	PAM4	128/64		234.375 MHz / 468.75 MHz		
High Speed Serial 50G	50G		128		390.625 MHz		
High Speed Serial 53.125G	53.125G				415.039 MHz		
High Speed Serial 56.25G	56.25G				439.45 MHz		
High Speed Serial 56G	56G				437.5 MHz		
JESD204C 24.75G	24.75G	NRZ	64		386.71875 MHz		
OTU1F	11.27008929G		64/32	156.25/312.5 MHz	176.0951 MHz / 352.19 MHz		
OTU1IB	10.71428571G				167.4107 MHz / 334.8214 MHz		
OTU2	10.70922532G				167.3316 MHz / 334.6633 MHz		
OTU2-HD	11.45571429G				178.9955 MHz / 357.9911 MHz		
OTU25	27.952493G		64		436.7577 MHz		
OTU25_RS	27.95249339G				436.7577 MHz		
OTU25u_RS	25.78165149G				402.8383 MHz		
OTU2E	11.09572785G		64/32		173.3707 MHz / 346.7415 MHz		
OTU50	55.904987G	PAM4	128		436.7577 MHz		
OTU50_RS	55.90498678G				436.7577 MHz		

Protocol Standard	SerDes Rate per Lane	PMA Electrical	PMA Width	Supported Reference Clocks	PMA Interface Frequency	PCS Data Path	Gearbox Mode
OTU50u_RS	53.12582732G				415.055 MHz		
OTUC1	56.15235398G				438.6903 MHz		
STM-64	9.95328G		64/32/20		155.52 MHz / 311.04 MHz / 497.664 MHz		
USB-C	20.625G		64		322.2656 MHz		
GPON/EPON	2.5G		40/32/20 /16		62.5 MHz/78.125 MHz/125 MHz/ 156.25 MHz		
PCIe-GEN1	2.5G	NRZ	40/20	100 MHz	62.5 MHz / 125 MHz	Pipe Mode, PCS bypass	8b/10b
PCIe-GEN2	5G				125 MHz / 250 MHz		
PCIe-GEN3	8G		64/32/16		125 MHz / 250 MHz / 500 MHz		128b/130b
PCIe-GEN4	16G		64/32		250 MHz / 500 MHz		
PCIe-GEN5	32G		64		500 MHz		

Chapter 4 : Speedster7t PCS Block

Introduction

The Achronix PCS serves as the conduit for the SerDes data path to and from the fabric. The PCS provides several options to encode, decode, bond lanes, and reorder bits. The PCS can be bypassed if none of the features are needed for the user design.

Three types of hard PCS controllers are offered within Speedster7t FPGAs:

- A PIPE5.1-compliant mode for PCIe.
- PCS bypass mode for direct use by the fabric.
- Gearbox mode for Ethernet, supporting 66/64 bit decoding or 67/64 bit decoding.

The raw SerDes PCS controller is covered in this section.

The Achronix PCS can support the rates and performance requirements for other protocols including CPRI, JESD204x and Interlaken. A soft controller is required in the fabric for these protocols. The Achronix PCS and PMA can be thought of as a unit. Some features in the PMA are controlled through the Achronix PCS. All lanes are configured as a quad, but can be used as a single lane or combined with other quads for a configurations that spans 16 lanes. Four quads are used to provided 16 high-speed lanes, two quads for eight lanes, and one quad for a four lane solution as shown in the following figure.

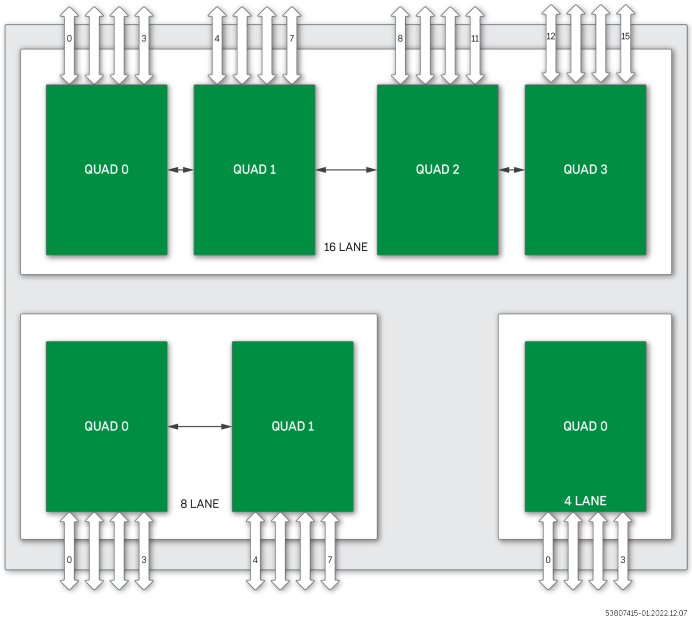

Figure 6 • SerDes Configurations

PCS Modes

The PCS has multiple modes:

- Ethernet Mode: The PCS is connected to a hard Ethernet MAC. This is covered in the ***Speedster7t Ethernet User Guide* (UG097)**[4].
- PCIe Mode: The PCS is connected to the hard PCIe Gen5 subsystem. This is covered in the *Speedster7t PCIe User Guide* (UG098) (support account required).
- Raw SerDes Mode: The PCS routes data directly to and from the fabric. In Raw Mode, there are three options for the data path. These options can be found in the ACE GUI under the **PCS Data Path** selector.

  Pipe Mode: The data is routed through a PCIe PIPE to enable soft controllers in the fabric, up to GEN4

  PCS Bypass Mode: The data is sent directly to/from the PMA to the fabric. All word alignment must be accounted for in the fabric.

  Gearbox Mode: The data is routed through the gearbox logic. The gearbox logic supports 66b/64b synchronous mode, 66b/64b asynchronous mode, and 67b/64b synchronous mode.

The following figure shows a high-level block diagram of the PCS and the RX/TX data multiplexing.

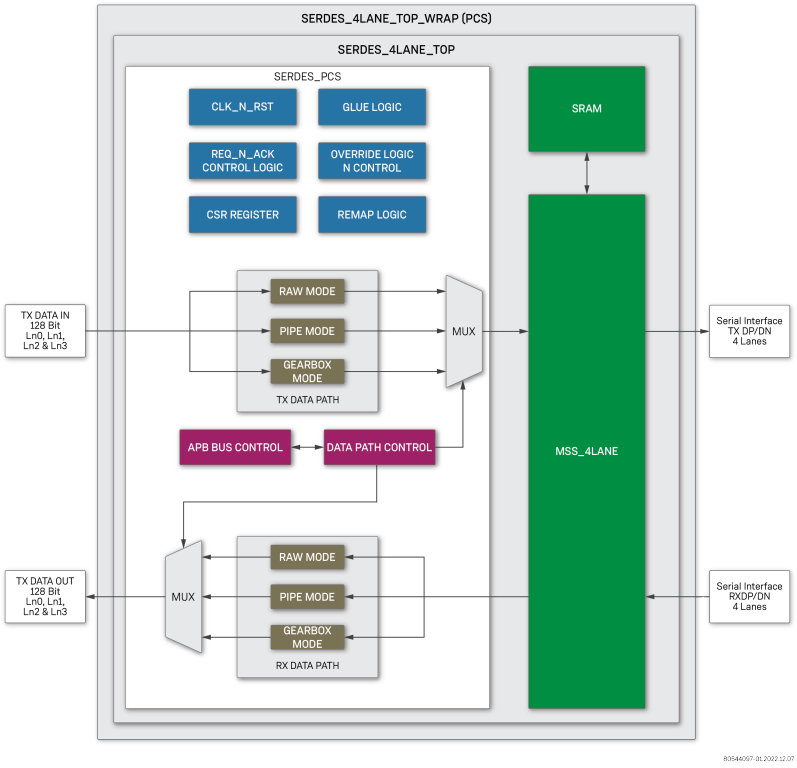

Figure 7 • PCS Modes

4 https://www.achronix.com/documentation/speedster7t-ethernet-user-guide-ug097

PCS Features

- 16/20/32/40/64/128 bit FPGA data path support
- PCIe protocol via the PIPE specification for implementation of a soft PCIe controller in the fabric:
  - 40-bit internal data path support for 8b/10b encoder path for PCIe Gen1/Gen2
  - Comma detection and byte/word alignment only for PCIe protocol 8b/10B alignment
  - 32-bit internal data path support for 128/130b encoder/decoder for PCIe Gen3/Gen4
  - Receive elastic FIFO is only for PIPE mode for clock compensation
- Support for bypassing the PCS for hard IP such as Ethernet Controller in the fabric
- Support for 66b/64b CAUI gearbox in both synchronous and asynchronous mode.
- Support for 67b/64b gearbox in synchronous mode only
- Protocols supported by the PMA via raw mode include:
  - Ethernet 1G/10G/25G/50G/100G/XAUI
  - CPRI
  - JESD204A/B/C
  - SyncE
  - Interlaken
- The PCS SerDes supports lane bonding up to 16 lanes using a quad as the basic lane bonding block

PCS SerDes Block Diagram

This section outlines the high-level hardware architecture block diagram of a quad lane SerDes (figure follows). The PCS SerDes IP consists of the following main functional blocks:

- PCS (transmitter and receiver)
- PMA (quad SerDes)

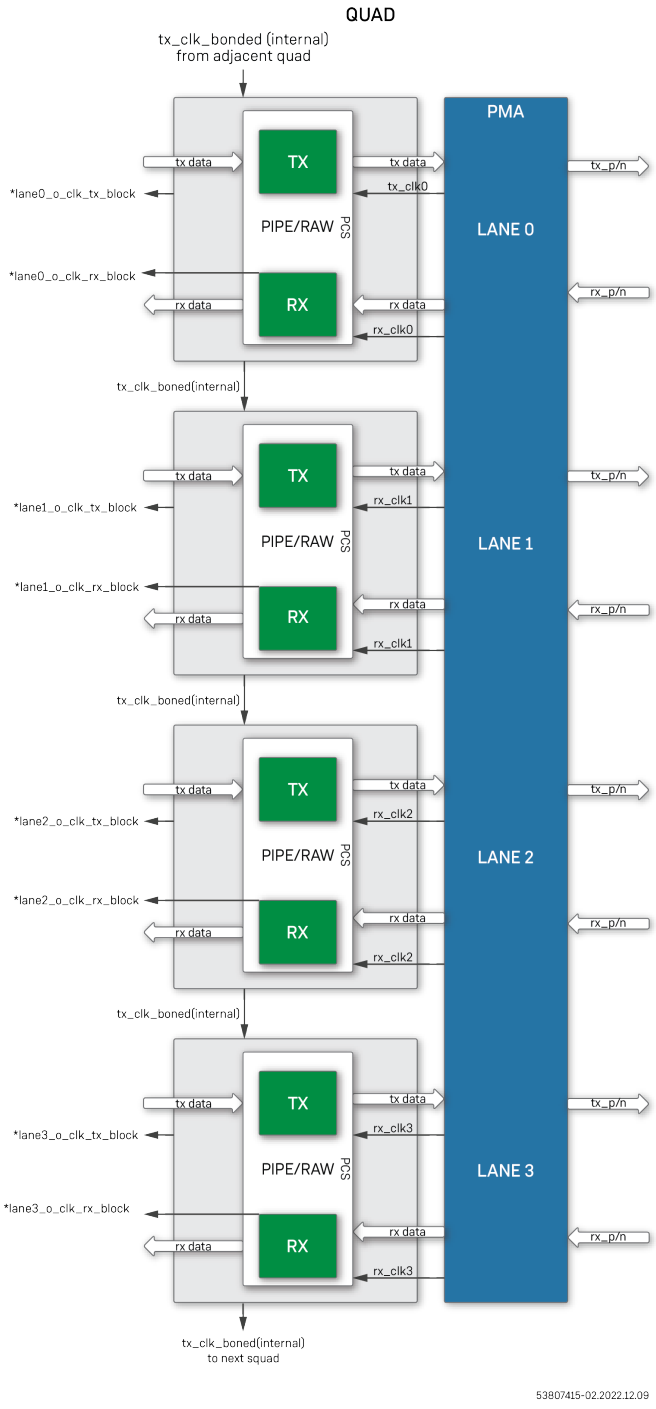

Figure 8 • Quad Transmit/Receive Path

Reference Clock Sharing

The following figure details sharing the reference clock between quads. The reference clocks can only be shared within a single ACXIP and must be within a single subsystem (ETHERNET_0, ETHERNET_1, or PCIE_1). An AXCIP is a configuration file created in ACE defining an IP configuration such as SerDes.

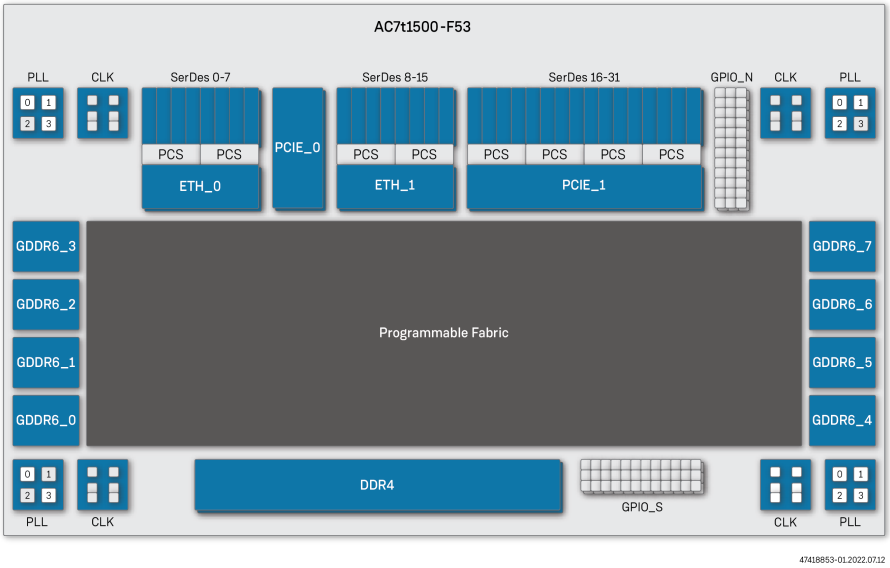

Figure 9 • Reference Clock Sharing

The following table details which lanes belong to each subsystem. Reference clock sharing is limited to lanes within a subsystem.

Table 9 • Reference Clock Sharing for AC7t1400/AC7t1500

Lanes	Subsystem	Reference Clock
3:0	ETHERNET_0	SRDS_N6_REFCLK_P
7:4	ETHERNET_0	SRDS_N7_REFCLK_P
11:8	ETHERNET_1	SRDS_N4_REFCLK_P
15:12	ETHERNET_1	SRDS_N5_REFCLK_P
19:16	PCIE_1	SRDS_N0_REFCLK_P
23:20	PCIE_1	SRDS_N1_REFCLK_P
27:24	PCIE_1	SRDS_N2_REFCLK_P

Lanes	Subsystem	Reference Clock
31:28	PCIE_1	SRDS_N3_REFCLK_P

PCS Transmit Architecture

The transmitter consists of the following four data paths. Each data path supports a particular encoding scheme which caters to a set of protocols.

- Transmit multiplexer logic
- 8b/10b encoding path (PCIe Gen1 and Gen 2)
- 128/130b encoding path (PCIe Gen3 and Gen 4)
- Transmit gearboxing (66b/64b and 67b/64b)
- PCS transmit direct path (16/20/32/40/64/128 bit)

Transmit Multiplexer Logic

The transmit multiplexer logic block performs the mode-dependent bit multiplexing. The supported modes are:

- Gearboxing
- PIPE (32 bit)
- Raw (128 bit)
- PRBS Generator

8b/10b Encoder

The 8b/10b encoder generates 10-bit code groups from 8-bit data and single-bit control input. The encoder uses the code group mapping specified in IEEE 802.3 clause 36. If the fabric interface uses a 32-bit data path, then four 8b/10b encoders are cascaded to produce a 40-bit code group output to the PMA for serialization. The 10-bit encoded output `tx_dataout[9:0]` maps to bits `{jhgf iedcba}` per the labeling used in IEEE 802.3-2005 clause 36. The encoder operates with four-byte data widths.

This block supports PCIe Gen1 and Gen2 in PIPE mode.

128b/130b Encoder Path

The 128b/130b encoder is specifically targeted at PCIe gen3/gen4. The interface is compliant with PIPE 5.1.

PCS Receive Architecture

The receiver consists of the following four data paths. Each data path supports a particular encoding scheme which caters to a set of protocols.

- Receive demultiplexer logic
- 8b/10b decoding (PCIe Gen1 and Gen 2)

- 128/130b decoding (PCIe Gen3-Gen5)
- 64b/66b and 64b/67b Gearboxing
- PCS receive direct path
- PRBS checker

Receive DeMUX logic

The receive deMUX logic block performs the mode-dependent bit demultiplexing. The supported modes are:

- Gearboxing (66b/67b)
- PIPE (32-bit)
- Raw (128 bit)

8b/10b Decoder Path

This path is used for implementing 8b/10b decoder-related receive path blocks. This path contains the following blocks:

- Comma detect and symbol alignment
- 8b/10b decoder
- Receive 8b/10b elastic buffer

Comma Detect and Symbol Alignment

The symbol alignment block can be configured to support a variety of standards by programming various characters. Currently supported standards are PCIe Gen 1 and Gen 2.

Symbol alignment is performed in automatic alignment mode only, using alignment and sequence characters for identifying the correct symbol boundary in the received data-stream. Attributes for alignment and sequence detect symbols are specified to be 10 bits wide. This block offers a programmable comma pattern with sequence options to fit any protocol or custom scenario.

8b/10b Decoder

The 8b/10b decoder generates 8-bit code groups and 1-bit control from 10-bit encoded data. It uses the code group mapping specified in IEEE 802.3 clause 36. If the fabric interface uses a 32-bit data path, then four 8B/10B decoders are cascaded to produce 32-bit data to the fabric. The decoder handles various error conditions reported on a per byte lane basis.

The running disparity should change polarity when a 6-bit or 4-bit code word with an unequal number of 0s and 1s is received. If reception of a 6-bit or 4-bit code word with an unequal number of 0s and 1s does not change the running disparity, a disparity error is asserted for the corresponding byte.

Any 10-bit code word that is not present in tables 36-1, 36-2 of the IEEE 802.3-2005 specification are considered as an invalid code word. In addition, the 11 code words corresponding to the K characters are programmable to be flagged as invalid code words. If the 10-bit code word happens to be present in tables 36-1 or 36-2, but corresponds to the wrong column (per the currently running disparity calculation), a wrong column indication is asserted.

Disparity and code errors are not mutually exclusive. However, code error and wrong column indication are mutually exclusive. For PCIe, if a code error and disparity error is detected on the same byte, the `pipe_rxstatus` is encoded to indicate a code error.

Receive 8b/10b Elastic Buffer

The 8b/10b elastic FIFO is used to synchronize the received data from the PMA-recovered clock to a system clock or local clock (typically transmit clock) in the 8b/10b encoding environment. This block operates in a 40-bit mode and provides a very generic programmable skip character detection.

The elastic FIFO compensates for the frequency offset by adding or deleting pre-configured skip characters from the received data stream. The elastic FIFO provides an indication that skip characters were added or deleted to the downstream logic. For PCIe, the elastic FIFO also includes the appropriate status encoding to indicate add/delete operation.

128b/130b Decoder Path

The 128b/130b decoder path is specifically targeted at PCIe Gen3-Gen4. The interface is compliant to PIPE 5.0 and consists of a block synchronizer and receives the Gen3-Gen4 elastic buffer.

Block Synchronizer

PMA parallelization occurs at arbitrary word boundaries. Consequently, the parallel data from the receive PMA CDR must be realigned to meaningful character boundaries. The PCI Express 4.0 base specification outlines that the data is formed using 130-bit blocks, with the exception of SKP blocks. A SKP ordered set can be 66, 98, 130, 162, or 194 bits long. The block synchronizer searches for the electrical idle exit sequence ordered set or skips (SKP) ordered set to identify the correct boundary for the incoming stream and to achieve block alignment. The block is realigned to the new block boundary following the receipt of a SKP ordered set, as it can be of variable length.

Receive Gen3-Gen5 Elastic Buffer

This elastic buffer compensates for small clock frequency differences between the recovered clock and the local clock domains by inserting or removing SKP symbols in the data stream to keep the FIFO from going empty or full respectively for PCIe Gen3/4/5 systems.

The PCI Express 4.0 base specification defines that the SKP ordered set (OS) can be 66, 98, 130, 162, or 194 bits long. The SKP OS has the following fixed bits: 2-bit Sync, 8-bit SKP END, and a 24-bit LFSR for a total of 34 bits. This block adds or deletes the 4 SKP characters (32 bits) to keep the FIFO from going empty or full, respectively. If the FIFO is nearly full, it deletes the 4 SKP characters (32 bits) by disabling write whenever a SKP is found. If the FIFO is nearly empty, the design waits for a SKP OS to start, then stops reading the data from the FIFO, and inserts a SKP in the outgoing data.

64b/66b and 64b/67b Bit Gearboxing

The receive gearbox is used to adapt the PMA data width to the width of the PCS-fabric interface. It supports different ratios (PMA interface width: fabric interface width) such as 64b/66b and 64b/67b. There are two modes supported:

- Synchronous mode – Supported for both 66 and 67 bit mode. The gearbox stalls the data throughput by de-asserting `data_valid` for one clock cycle to match the ratio. The fabric receives a `data_valid` signal along with the data which must be monitored.
- Asynchronous mode – Supported only for 66 bit mode. The gearbox provides the data on each clock cycle of the receive clock. Data is valid on every clock cycle in asynchronous mode.

Gearbox Mode

The transmit gearbox is used to adapt the PCS data width to the width of the PCS-PMA interface. The gearbox supports different ratios (fabric interface width: PMA interface width) such as 66b/64b (synchronous and asynchronous) and 67b/64b (synchronous). This block can either operate seamlessly based on two clocks with different rates 66b/64b, or operate on a single clock with wait states added during the gearbox wrap around time for 67b/64b (synchronous mode).

Gearboxing Implementation

Clocking and Usage

The following figure shows the clock and data path for a gearboxing implementation in the PCS for a quad.

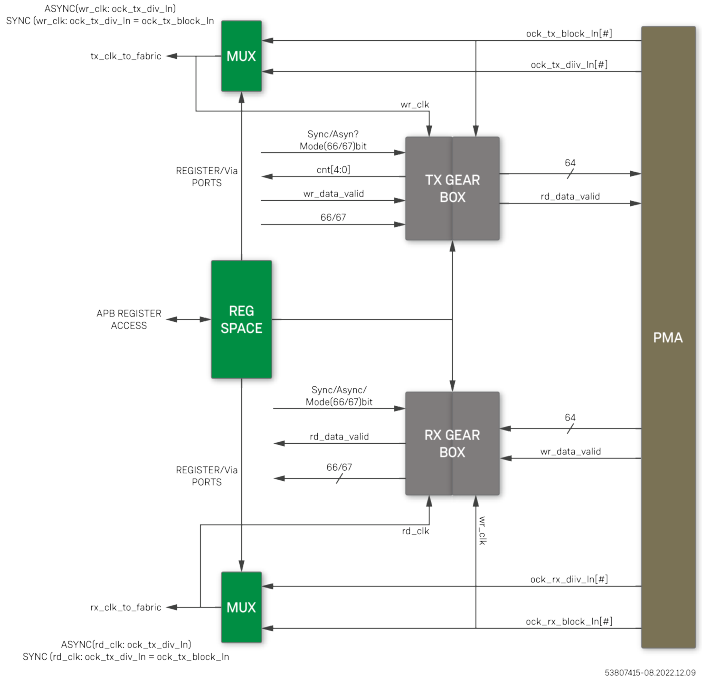

Figure 10 • Gearbox Implementation

Gearbox Ports Mapping

Table 10 • Gearbox Transmit Data Port Mapping

Port	Gearbox Port Name/Usage	Width
i_tx_data[66:0]	67/66 bit data input.	67
i_tx_data[67]	Enable 66-bit asynchronous gearbox.	1
i_tx_data[68]	Enable 66-bit synchronous gearbox.	1
i_tx_data[69]	data valid.	1
i_tx_data[70]	Enable 67-bit synchronous gearbox.	1
i_tx_data[77:71]	7-bit synchronous counter.	7

Table 11 • Gearbox Receive Data Port Mapping

Port	Gearbox Port Name/Usage	Width
o_rx_data[66:0]	67/66 bit output data.	67
o_rx_data[67]	Indicates skip missed for synchronous gearbox.	1
o_rx_data[68]	Rx data valid.	1

PIPE Mode

The PIPE mode enables access to the PCS PIPE 5.1-compliant interface. The PCS layer supports PCIe Gen4 in PIPE mode using a soft controller in the fabric. The following diagram details the various supported combinations of clock and data width when the PCS supports PCIe.

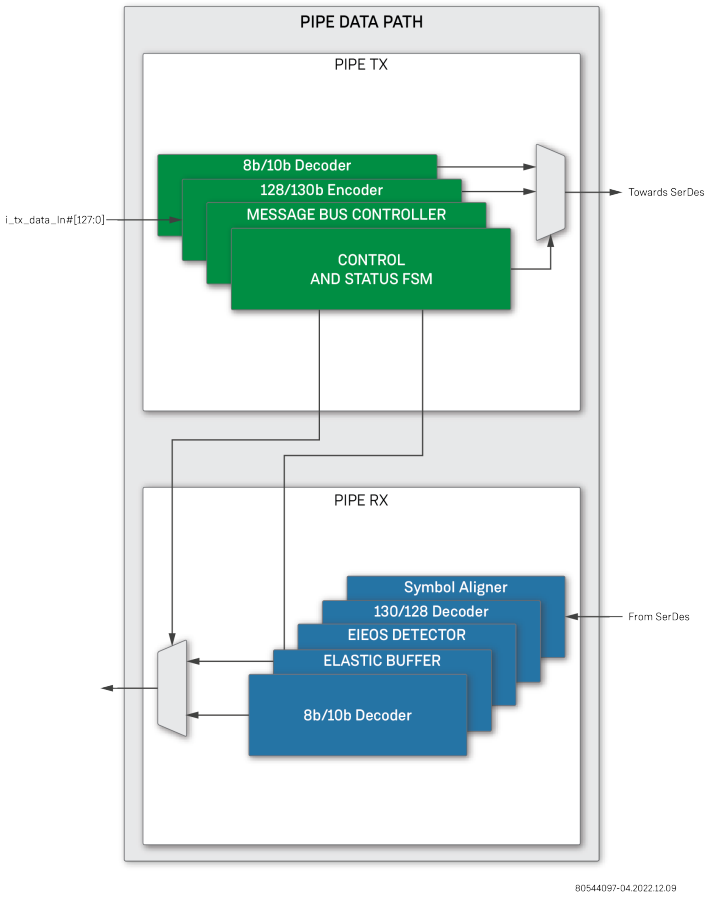

Figure 11 • PCIe PIPE Mode Clock and Data Width

Rates

The PCS layer includes the glue logic to switch the PMA data width to 32-bit mode and program the final rate bits for PCIe gen3/gen4 operation. The following table lists the various supported combinations of clock and data width when the PCS supports PCIe.

Table 12 • PCIe Generation with PCLK Rates and Supported Data Widths

PCIe Mode	PCLK	PMA Data Width
2.5 Gbps Gen1	62.5 MHz	40 bits
5.0 Gbps Gen2	125 MHz	
8.0 Gbps Gen3	250 MHz	32 bits

PCIe Mode	PCLK	PMA Data Width
16.0 Gbps Gen4	500 MHz	

PIPE Ports Mapping

Table 13 • PIPE Mode Transmit Data Port Mapping

Port	PIPE Port Name	Width	Description
i_tx_data[31:0]	TxData	32	Transmit PIPE Data.
i_tx_data[70:67]	TxElecidle	4	Transmit electrical idle forces tx_p/n to idle state.
i_tx_data[72:71]	TxSubsample	2	Not Supported.
i_tx_data[73]	TxBeaconEnable	1	Enable transmit of a Beacon. 1 Beacon transmit is enabled, 0 Beacon transmit is disabled.
i_tx_data[77:74]	TxDataK	4	These signals indicate the type of characters on the TxData bus. A 1'b0 indicates a data character; while a 1'b1 indicates a control character. • i_tx_data[74] - TxData[7:0] • i_tx_data[75] - TxData[15:8] • i_tx_data[76] - TxData[23:16] • i_tx_data[77] - TxData[31:24]
i_tx_data[78]	TxDataValid	1	TxDataValid qualifies the data on the TxData bus and is active high.
i_tx_data[80:79]	TxSyncHeader	2	For Gen3 operation. Specifies the receive block type: • 2'b01: Ordered Set Block • 2'b10: Data Block These signals can be grounded if the design is not targeting Gen3.
i_tx_data[81]	TxStartBlock	1	Allows the MAC to tell the PHY the starting byte for the 128b block, active high. The starting byte for a 128b block must always start with byte 0 of the data interface.

Port	PIPE Port Name	Width	Description
i_tx_data[82]	TxCompliance	1	Used when transmitting the PCI Express compliance pattern, active high. This signal is sampled on TxDataValid.
i_tx_data[83]	SRISEnable	1	Not Supported.
i_tx_data[91:84]	M2PMessageBus	8	The MAC multiplexes command, and required address, and any required data for sending read and write requests to access PHY PIPE registers and for sending read completion responses and write ack responses to PHY initiated requests. Refer PIPE spec 5.1 message bus section for full definition.
i_tx_data[92]	RXEiDetectDisable	1	Not Supported.
i_tx_data[93]	TxCommonModeDisable	1	Not Supported.
i_tx_data[94]	PclkChangeAck	1	Not Supported.
i_tx_data[95]	AsyncPowerChangeAck	1	Not Supported.
i_tx_data[96]	TxDetectrx/Loopback	1	Used to tell the PHY to begin a receiver detection operation or to begin loopback, active high.
i_tx_data[100:97]	PowerDown	4	Power the transceiver up or down. Power states: 4'b0000 – P0 normal operation. 4'b0001 – P0 low recovery time latency, power saving state. 4'b0010 – P1 longer recovery time latency, lower power state. 4'b0011 – P2 lowest power state. 4'b0100 – PD (full power down).
i_tx_data[103:101]	TxRate	3	Control the link symbol rate: 3'b000 – 2.5 GB/s symbol rate. 3'b001 – 5.0 GB/s symbol rate. 3'b010 – 8.0 GB/s symbol rate. 3'b011 – 16.0 GB/s symbol rate.
i_tx_data[106:105]	Width	2	Fixed to 32 bit.

Port	PIPE Port Name	Width	Description
i_tx_data[111:107]	PclkRate	5	Not Supported.
i_tx_data[112]	RxStandby	1	Not Supported.
i_tx_data[113]	MsgbusRstn	1	Reset the message bus, active low.

Table 14 • PIPE Mode Receive Data Port Mapping

Port	PIPE Port Name	Width	Description
o_rx_data[31:0]	RxData	32	Received PIPE data.
o_rx_data[66-32]	Unused.	35	Unused.
o_rx_data[67]	RxSignalDetect	1	Indicates presence of a signal at the receiver input.
o_rx_data[68]	RxValid	1	Indicates symbol lock and valid data on RxData and RxDataK and further qualifies RxDataValid when used. Active high.
o_rx_data[69]	RxElecidle	1	Receiver detection of an electrical idle. Indicates detection of a beacon in PCIe mode. Active high.
o_rx_data[70]	PHYStatus	1	Communicates the completion of a stable clock after any change in state (power state transition, rate change, reset, or receiver connection). Active high.
o_rx_data[74:71]	RxDataK	4	Data/Control bit for the symbols of receive data. A value of 1 indicates a control byte. • o_rx_data[71] = RxData[7:0] • o_rx_data[72] = RxData[15:8] • o_rx_data[73] = RxData[23:16] • o_rx_data[74] = RxData[31:24]
o_rx_data[75]	RxDataValid	1	Indicates RxData is valid, active high.

Port	PIPE Port Name	Width	Description
o_rx_data[78:76]	RxStatus	3	Receive status and error from the PHY to the MAC. • 3'b000 – Receive Data Ok. • 3'b001 – SKP added. • 3'b010 – SKP removed. • 3'b011 – Receiver detected. • 3'b100 – 8b/10b, 128b/130b decode error. • 3'b101 – Elastic buffer overflow. • 3'b110 – Elastic buffer underflow. • 3'b111 – Receive disparity error.
o_rx_data[79]	RxStandbyStatus	1	Not Supported.
o_rx_data[81:80]	RxSyncHeader	2	Sync header for the MAC to use with the next 128b block. The MAC reads this value when the RxStartBlock signal is asserted.
o_rx_data[82]	RxStartBlock	1	Used at the 8.0 GB/s and 16 Gb/s PCI Express signaling rates, active high. The signal allows the PHY to tell the MAX the starting byte for a 128b block. The starting byte for a 128b block must always start with byte 0 of the data interface.
o_rx_data[90:83]	P2MMessagebus	8	The PHY multiplexes command, required address, and any required data for sending read and write requests to access MAX PIPE registers and for sending read completion responses and write ack responses to MAX-initiated requests. Refer to the PIPE 5.1 spec for message bus definitions.
o_rx_data[92:91]	DataBusWidth	2	Fixed to 32 bit.
o_rx_data[93]	RefClkRequired	1	Not Supported.
o_rx_data[94]	PclkChangeOk	1	Not Supported.

Note

It is the responsibility of the user to implement the deskew and CDC-related implementation in the fabric.

Chapter 5 : Speedster7t SerDes Register Map

Introduction

In order to support configuration and status monitoring of the SerDes subsystem, the control and status registers (CSR) are located within the overall device memory map. These register can be accessed through a number of mechanisms, including:

- PCIe subsystem
- JTAG port
- `NAP_AXI_MASTER` instantiated in the programmable fabric

For more general information about the device register space, see ***Runtime Programming of Speedster FPGAs (AN025)***[5].

Control and Status Registers

The Speedster7t FPGA control and status registers (CSR) are programmable and observable. This includes registers in the SerDes PHY. The key organizational principle of the register space is the subdivision of registers into common and lane-specific registers. Common registers apply to both the common lane of the quads and SerDes PHY functions that are shared across all of the lanes. Lane-specific registers contain the configuration and status information for a specific lane (e.g., Lane0)

CSRs serve a number of different functions in the design, including:

- Configuration registers, where the register provides the only means to set up advanced functionality or behaviors within the SerDes PHY
- Status registers, where the register provides the only means of observing a specific status signal
- SerDes PHY/Fabric interface to override registers, allowing the SerDes PHY interface outputs and/or inputs to be overridden to permit system-level debug
- Observability of registers for debug (additional observability is possible via the SerDes test/trace bus)

Global Address Space

CSR Addressing

The Speedster7t device supports a 42-bit address region. Within that address region, bits [41:34] define the top level spaces. The CSR space is defined as shown in the following table.

5 https://www.achronix.com/documentation/runtime-programming-speedster-fpgas-an025

Table 15 • Speedster7t FPGA Global Address Map

Address Bit	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	...	0
CSR Space	0	0	1	0	0	0	0	0	Target ID						IP ID				Register Address			

Target ID Addressing

The raw SerDes lanes are a subset of the Ethernet and PCIE target IDs. Each SerDes quad is associated with one of the following Target IDs (address bits [33:28]):

Table 16 • SerDes Target ID Address Map

Target ID							Description
CSR Space	**33**	**32**	**31**	**30**	**29**	**28**	
Ethernet 0	0	1	1	0	1	1	Ethernet 0, SerDes 0 (lanes[3:0]) Ethernet 0, SerDes 1 (lanes[7:4])
Ethernet 1	0	1	1	1	0	0	Ethernet 1, SerDes 0 (lanes[11:8]) Ethernet 1, SerDes 1 (lanes[15:12])
PCIE 1	0	1	1	0	0	1	PCIE 1, SerDes 0 (lanes[19:16]) PCIE 1, SerDes 1 (lanes[23:20]) PCIE 1, SerDes 2 (lanes[27:24]) PCIE 1, SerDes 3 (lanes[31:28])

IP ID Addressing

Each SerDes quad has a unique IP ID under the quad target ID. The `IP_ID` address field (address bits [27:24]) is defined as follows:

Table 17 • Ethernet IP ID Address Map

IP ID					Description
CSR Space	**27**	**26**	**25**	**24**	

SerDes Quad 0	1	0	0	0	Ethernet 0, SerDes Quad 0 (lanes 3-0). Ethernet 1, SerDes Quad 0 (lanes 11-8). PCIE 1, SerDes Quad 0 (lanes 19-16).
SerDes Quad 1	1	0	0	1	Ethernet 0, SerDes Quad 1 (lanes 7-4). Ethernet 1, SerDes Quad 1 (lanes 15-12). PCIE 1, SerDes Quad 1 (lanes 23-20).
SerDes Quad 2	1	0	1	0	PCIE 1, SerDes Quad 2 (lanes 27-24).
SerDes Quad 3	1	0	1	1	PCIE 1, SerDes Quad 3 (lanes 31-28).

Address Dictionary Tokens

To simplify access to the device memory space, there is an address dictionary which divides the memory areas into tokens. This dictionary is used to access memory areas and individual registers using names, rather than direct addresses. This token approach results in more readable code while reducing the need to remember individual addresses.

The address dictionary is included as part of ACE, accessed using the Tcl console, and used to access the memory space via the JTAG port. The tokens for the SerDes subsystems address areas listed in the above table are as follows:

Table 18 • Address Dictionary Tokens

Top Level	Target ID	IP ID	SerDes Lanes
CSR_SPACE	ETHERNET_0	SERDES_0	[3:0]
	ETHERNET_0	SERDES_1	[7:4]
	ETHERNET_1	SERDES_0	[11:8]
	ETHERNET_1	SERDES_1	[15:12]
	PCIE_1	SERDES_0	[19:16]
	PCIE_1	SERDES_1	[23:20]
	PCIE_1	SERDES_2	[27:24]
	PCIE_1	SERDES_3	[31:28]

For more information on how to use the Address dictionary tokens refer to ***Runtime Programming of Speedster FPGAs*** **(AN025)**[6].

Register Address Within the SerDes

The Register Address, bits [23:0], of each SerDes quad is broken down into three subsystems: PMA, PCS Common, and PCS lane-specific registers. Within each of those subsystems, bits [19:0] can be used to address registers within those subsytems.

Table 19 • SerDes Subsystem Register Addressing

Level	Subsystem	Register Address[23:20]
SerDes PHY	PMA	4'b0000
	PCS Common	4'b1011
	PCS Lane[0]	4'b1100
	PCS Lane[1]	4'b1101
	PCS Lane[2]	4'b1110
	PCS Lane[3]	4'b1111

Register Address, PMA Subsystem

The Register Address space of the PMA system can be broken down further than that shown above. If the PMA subsystem is selected (bits[23:20] = 4'b0000), the remaining bits are defined as shown in the following table.

Table 20 • SerDes PMA Subsystem Register Addressing

Address Bit	23	22	21	20	19	18	16	15	14	13	...	0
PMA Subsystem Address	0	0	0	0	SRAM	Broadcast	PMA lane			Register offset		

6 https://www.achronix.com/documentation/runtime-programming-speedster-fpgas-an025

SRAM: Bit[19]

Bit 19 selects the static RAM of the PMA quad. The PMA requires loading of the instruction set into the SRAM upon the device bring-up. The SRAM space holds the customer-defined preset rate configurations. These presets are typically part of the IP setup in ACE and written at initial configuration.

Broadcast: Bit[18]

Bit 18 selects broadcast mode for the PMA quad. In broadcast mode, the register offset location of each of the four lanes is written with the desired value.

Lane: Bit[16:14]

When not in broadcast mode, Bits [16:14] select the lane of the PMA quad being written to or read from.

Table 21 • SerDes PMA Subsystem Quad Lane Addressing

Level	PMA Lane	Bits [16:14]
PMA Lane	Common	3'b000
	Lane 0	3'b001
	Lane 1	3'b010
	Lane 2	3'b011
	Lane 3	3'b100

Chapter 6 : Speedster7t SerDes IP Software Support in ACE

Introduction

The ACE GUI supports configuration of the Speedster7t SerDes in raw mode. Within ACE, the IP can be configured and added to the project. ACE also supports generating the timing files, pin constraints, bitstream files, and simulation files. These files are necessary for simulation and place/route. The following sections describe how to configure the SerDes subsystem in Raw Mode and generate the necessary files within the ACE environment.

More details on the usage of the ACE tool can be found in ***ACE User Guide*** **(UG070)**[7].

SerDes IP Configuration

SerDes IP configuration consists of the following steps:

New SerDes IP Instantiation

1. From an open project, right click the IP folder under the project name and select New IP Configuration.
2. In the New IP Configuration dialog, select Raw SerDes and assign a proper file name for the new IP (i.e., `raw_serdes_1.acxip`). Click **Finish** to complete the process.

A new IP with the given name `raw_serdes_1.acxip` appears in the IP folder.

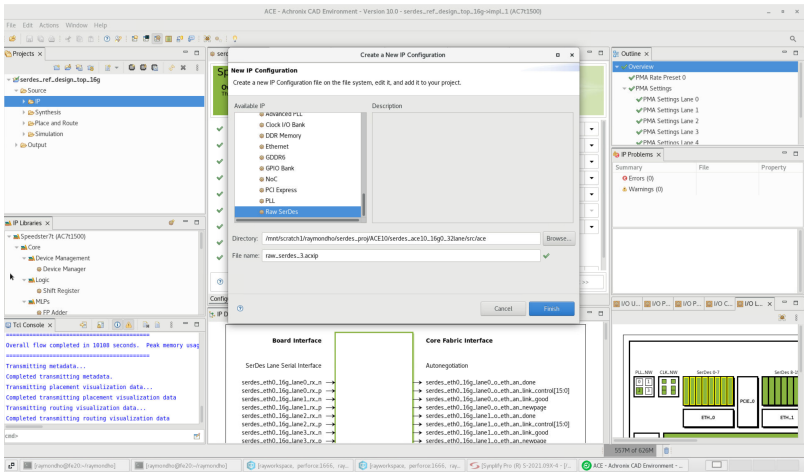

Figure 12 • Adding a New Raw SerDes Block

7 https://www.achronix.com/documentation/ace-user-guide-ug070

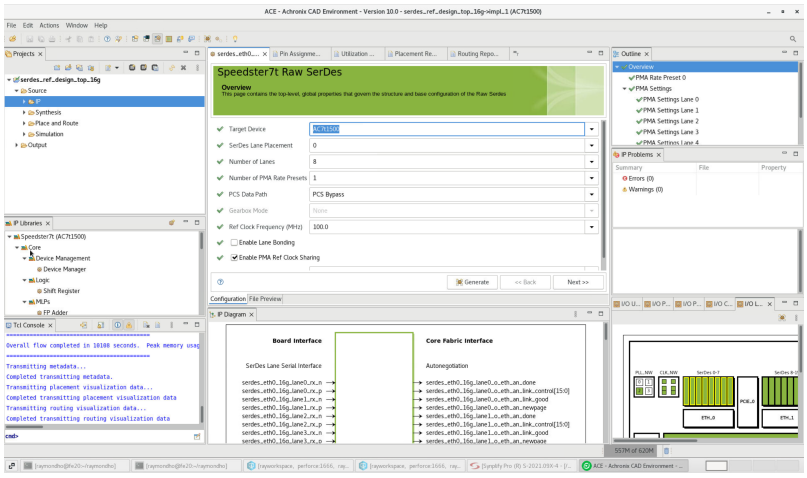

Figure 13 • Enable PMA SerDes Reference Clock Sharing

New SerDes IP Configuration

1. In IP Configuration Perspective view, click the new SerDes IP, `raw_serdes_1.acxip` under the IP folder. The Speedster7t Raw SerDes Overview window opens. This window is where the Raw SerDes properties and parameters are configured. In this example, a single lane IP with 100MHz reference clock and a symbol rate of 2.5G (PCIe Gen1) is configured.
2. Set the Target Device to AC7t1500.
3. Open the SerDes Lane Placement listbox and select the lane number where the new SerDes IP will be placed. In this example, Lane 0 is selected.

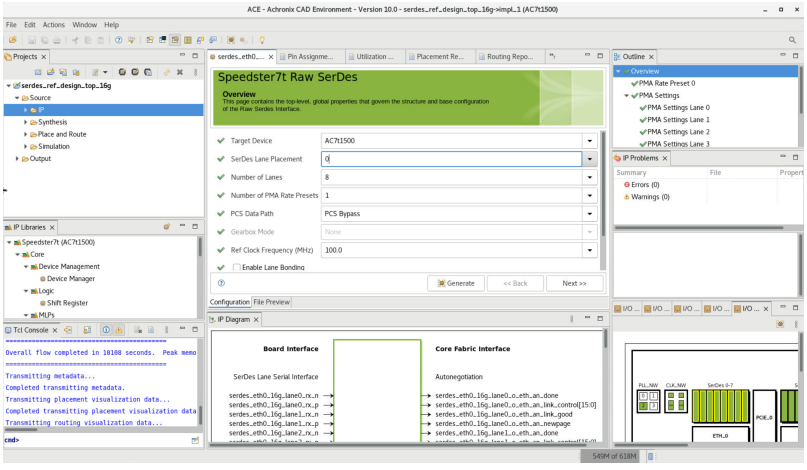

Figure 14 • SerDes Lane Placement

4. Open the Number of Lanes listbox and choose the number of lanes for the SerDes IP. The maximum number of lanes allowed is 16. In this example, the IP will be one lane wide.

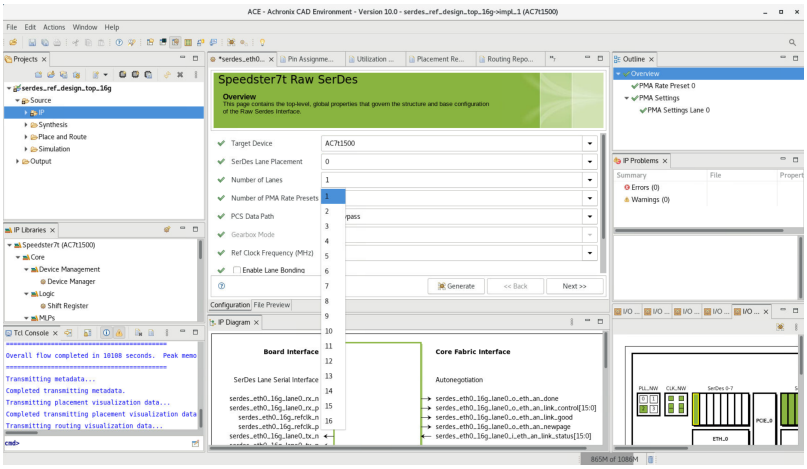

Figure 15 • Setting the Number of Lanes for the Block

5. Open the Number of PMA Rate Presets listbox and select the number of preset data rates for the new SerDes IP. This selection determines the number of rate configurations that are preprogrammed into the device at power up. The maximum number of preset rates is 8. In this example, one preset rate is selected. If multiple rates are selected, the device powers up to "PMA Rate Preset 0". Details on how to change rates during runtime can be found in the Example of TCL Scripts

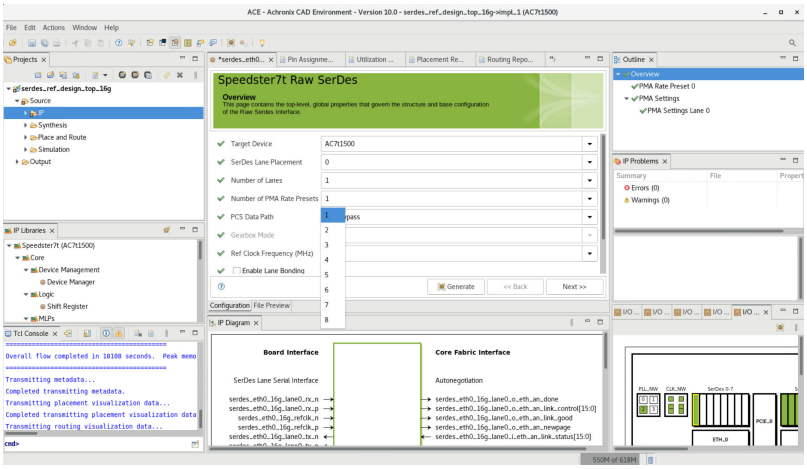

Figure 16 • Set Number of PMA Rate Pre-set

6. In the PCS Data Path listbox, select PCS Bypass mode for the new SerDes IP. This allows a direct connection between the SerDes and the logic in the fabric. Pipe Mode selects the PHY interface for he PCI Express and Gearbox Mode provides access to the gearbox modes.

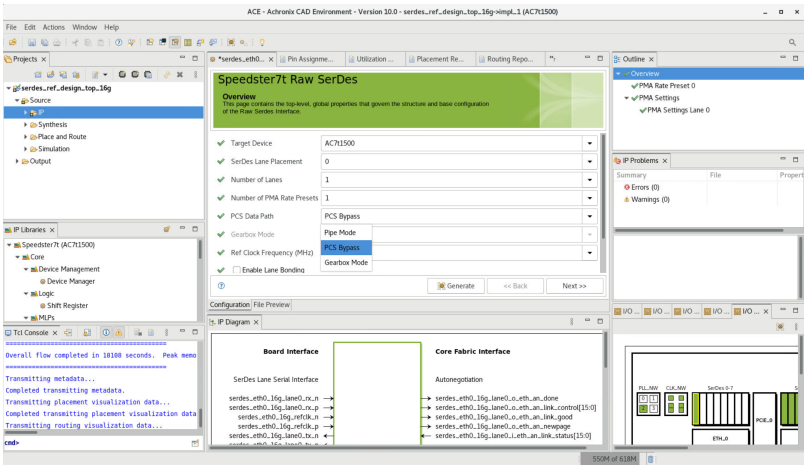

Figure 17 • Setting the Number of PMA Rate Pre-set

7. Select the clock frequency that is being driven to the reference clock pin. This example is using lane zero, so reference clock `SRDS_N6_REFCLK_P/N` is applicable. This example assumes 100 MHz is being driven to that pin.

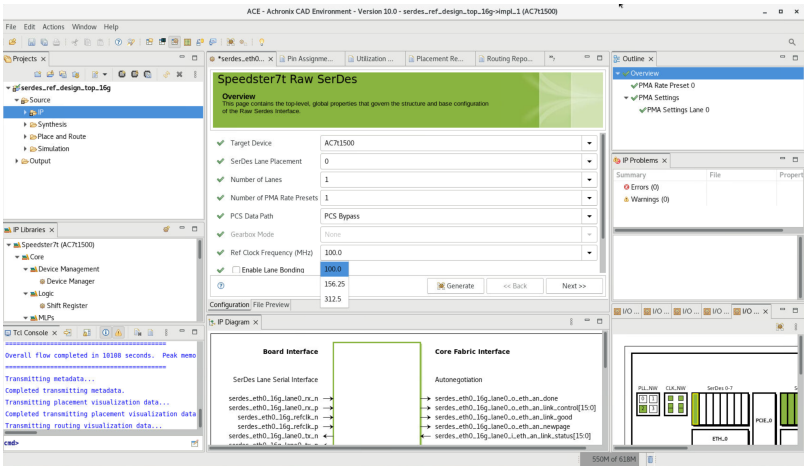

Figure 18 • Setting the SerDes Input Reference Clock Rate

8. An external reference clock is required for the SerDes IP. The PMA Ref Clock Sharing function is not enabled for this design because it is a single lane. If the ACXIP spans multiple quads, the Ref Clock Sharing Function can be enabled and the ref clock can be shared across the quads. Click **Next** to continue the configuration process.
9. The necessary protocol can be selected to meet system requirements. The Ref Clock Frequency dictates which protocols can be selected. The Protocol Standard, PCIe Gen1, is used in this example. After selection, the resulting Symbol Rate is shown.

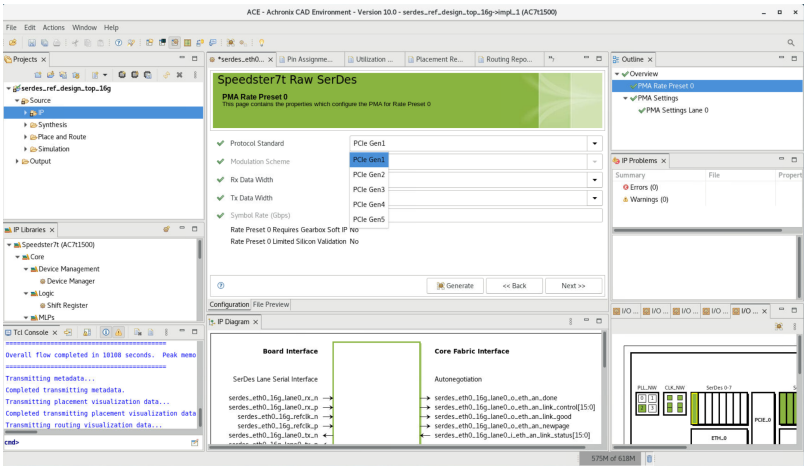

Figure 19 • Setting SerDes Input Reference Clock Rate

10. The data width chosen affects the speed at which the fabric/IORING interface needs to run to meet the protocol symbol rate. The Rx Data Width and Tx Data Width are both selected to be 40 in this example. A selection of 20 would require the IORING fabric interface to run at twice the rate.

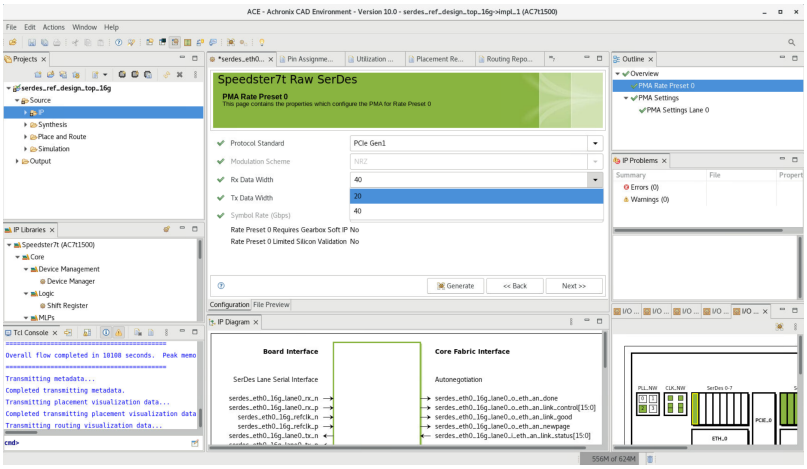

Figure 20 • Setting the Receive and Transmit Data Widths

11. **PMA power state** selects the mode in which the PMA is initialized. **P0 Normal Mode** is the normal, full operational mode and is selected in this example. Details on the other available power states can be found in the PMA section (page 9).

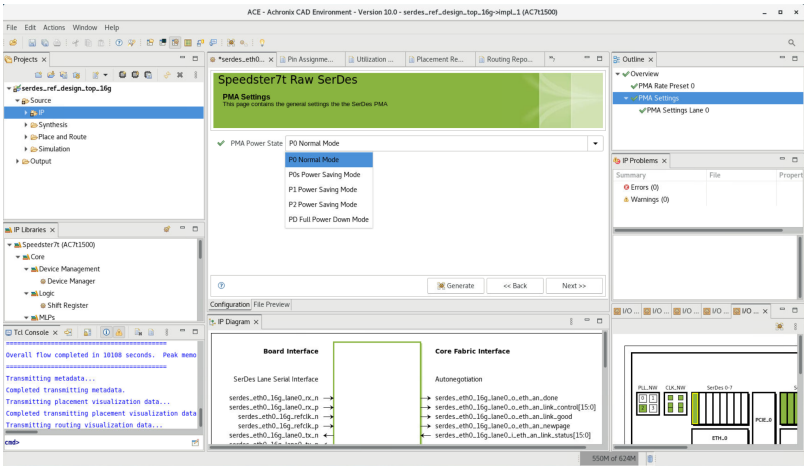

Figure 21 • Setting the PMA Power State

12. The TX driver settings are preset for each protocol. It is recommended to keep these values at their default settings. Details on the available driver options can be found in the PMA section (page 9).

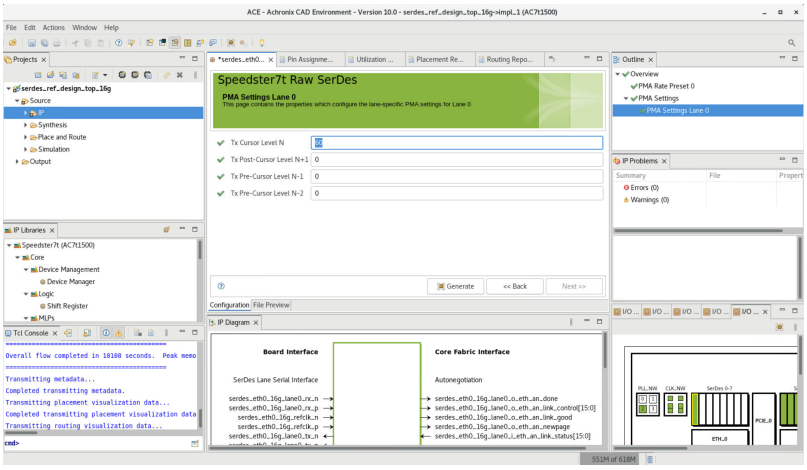

Figure 22 • Setting the Default Transmit Equalization

13. Click the **Generate** button. This action starts the process that generates the collateral needed by simulation and by ACE for the hardware implementation. The files are generated in a folder chosen by the user. The default location, `<implementation_directory>/ioring_design`, is shown in the example as `tmp/example_designs/ioring_design`. The constraint files and bitstream files needed by ACE are added to the project automatically if **Add to active project** is selected.

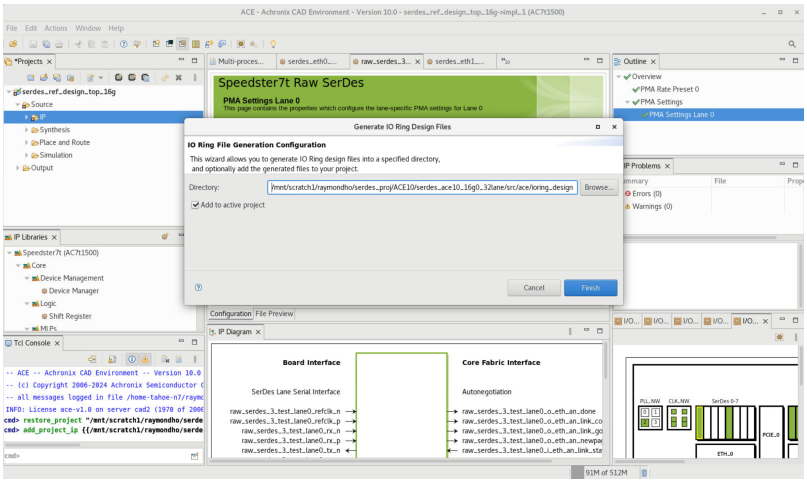

Figure 23 • Specified the I/O Ring design files directory.

14. The interface pins and signals for the new SerDes IP are displayed In the IP Diagram widow. These signals are written to a text file during the generate step. This file is called `<project_name>_user_design_port_list.svh`. In this example, the files name is `serdes_ref_design_top_2g5_user_design_port_list.svh`. The port list in the top-level RTL must match this list exactly.

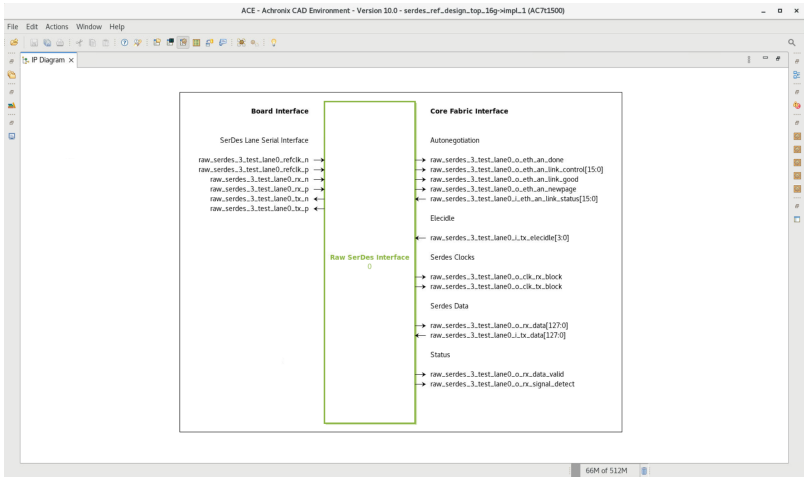

Figure 24 • New IP Interface Pins and Signals.

This concludes the creation of a raw SerDes block. A detailed example can be found in the *Speedster7t SerDes Reference Design Guide* (RD029).

Chapter 7 : Speedster7t FPGA SerDes Monitor (Eye Plot)

The receive channel of the SerDes block has an on-chip eye monitor function. It is a non-destructive eye monitor for lane diagnostics and debugging without disturbing the traffic. The eye plot function is a built-in function of the ACE Tool Suite, and can be executed at ACE GUI or Tcl console.

Software Requirement

The eye diagram plot tool is a third-party tool. For ACE9.2.1 or later revision, Matlab Runtime R2021b(9.11) installation is required. The Matlab Runtime can be downloaded from **www.mathworks.com/products/compiler/matlab-runtime**[8]

Method 1 (ACE GUI)

1. Set Jtag ID: Open the ACE project → tcl console

```
set jtag_id xxxxx
```

2. Open the Jtag port and connect the device.

```
ac7t1500::open_jtag
```

3. Open the ACE project → "I/O layout Diagram" → Right-click the SerDes instance and select "Plot SerDes Diagram"

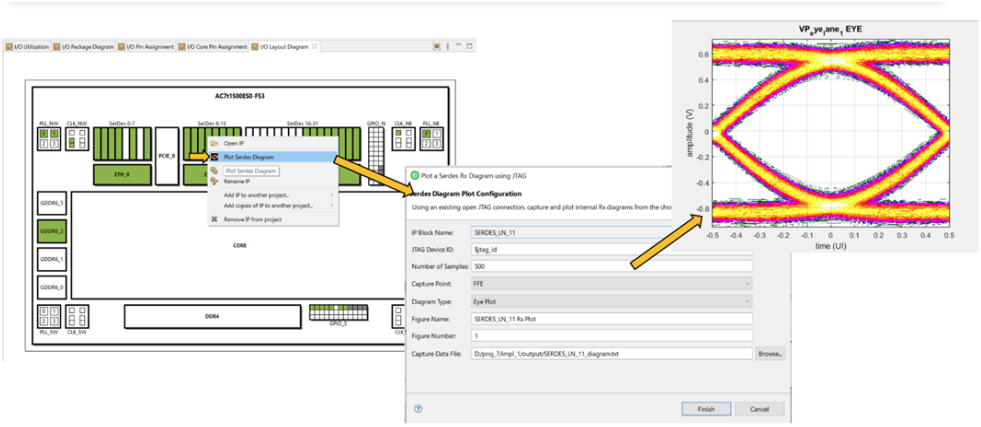

Figure 25 • Plot SerDes Diagram

8 https://www.mathworks.com/products/compiler/matlab-runtime.html

> **Note**
> The minimum sample rate is 100 samples.

Method 2 (Tcl Commands):

The eye diagram plot uses different commands for NRZ and PAM4 modulation. See eye diagram plot example code for NRZ and PAM4 modulation at step 4.

1. Set JTAG ID. Open the ACE project → tcl console and enter:

```
set jtag_id xxxxx
```

2. Open the JTAG port and connect the device.

```
ac7t1500::open_jtag
```

3. Read the sample data from the eye monitor and save it to a text file.

```
#jtag::capture_serdes_diagram_data <jtag_id> <subsystem> <serdes_quad> <serdes_lane>
-num_samples <int> -capture_point <string> -output_file <string>
#<jtag_id>                : The unique ID of JTAG devices to communicate with
#<subsystem>              : One of PCIE_1/ETHERNET_0/ETHERNET_1
#<serdes_quad>            : One of SERDES_0/SERDES_1/SERDES_2/SERDES_3
#<serdes_lane>            : One of 0/1/2/3
#[-output_file <string>]  : Optional file to output captured data results.
#[-num_samples <int>]     : Number of samples. Default: 500.
#[-capture_point <string>]: One of FFE/ADC/DCOFFSET. Default:FFE

Example:
jtag::capture_serdes_diagram_data $jtag_id "PCIE_1" "SERDES_3" "3" -num_samples 500
 -capture_point "FFE" -output_file "my_ffe_output.txt"
```

4. Call MatLab Runtime Plot:

Eye Plot for NRZ Modulation

```
#jtag::plot_serdes_diagram_data_matlab <input_file> <diagram_type> <mod>
<figure_name> <figure_number> <rate>
#<input_file>           : The file containing the data results from
jtag::capture_serdes_diagram_data
#<diagram_type>         : Diagram type. Choose one of: eye/bathtub/hist
#<mod>                  : Mod type. Choose one of: NRZ/PAM4
#<figure_name>          : Name to identify the figure
#<figure_number>        : Number to identify the figure
```

```
#<rate>                  : Baud rate

Example:
jtag::plot_serdes_diagram_data_matlab "my_ffe_output.txt" "eye" "NRZ" "my_plot" "1"
"15e9"
```

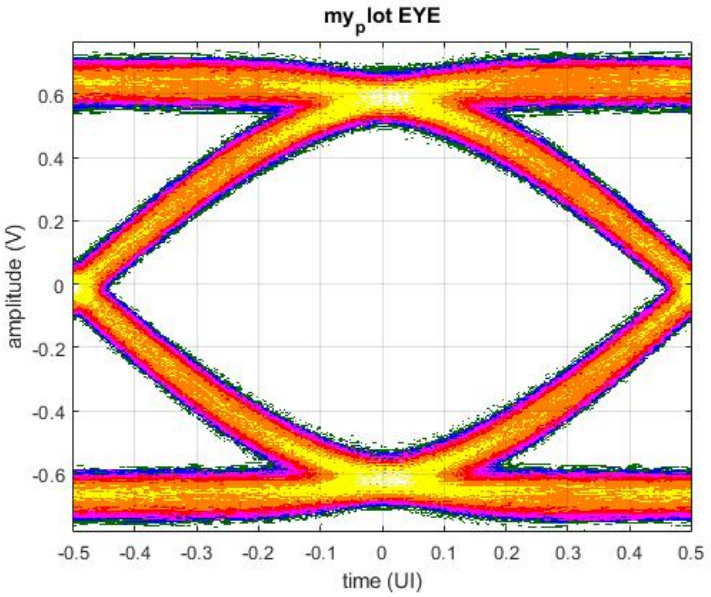

Figure 26 • Eye Diagram of NRZ

Eye Plot for PAM4 Modulation

```
#jtag::plot_serdes_diagram_data_matlab <input_file> <diagram_type> <mod> <figure_name>
<figure_number> <rate>
#<input_file>            : The file containing the data results from
jtag::capture_serdes_diagram_data
#<diagram_type>          : Diagram type. Choose one of: eye/bathtub/hist
#<mod>                   : Mod type. Choose one of: NRZ/PAM4
#<figure_name>           : Name to identify the figure
#<figure_number>         : Number to identify the figure
#<rate>                  : Baud rate

Example:
jtag::plot_serdes_diagram_data_matlab "my_ffe_output.txt" "eye" "PAM4" "my_plot" "1"
"15e9"
```

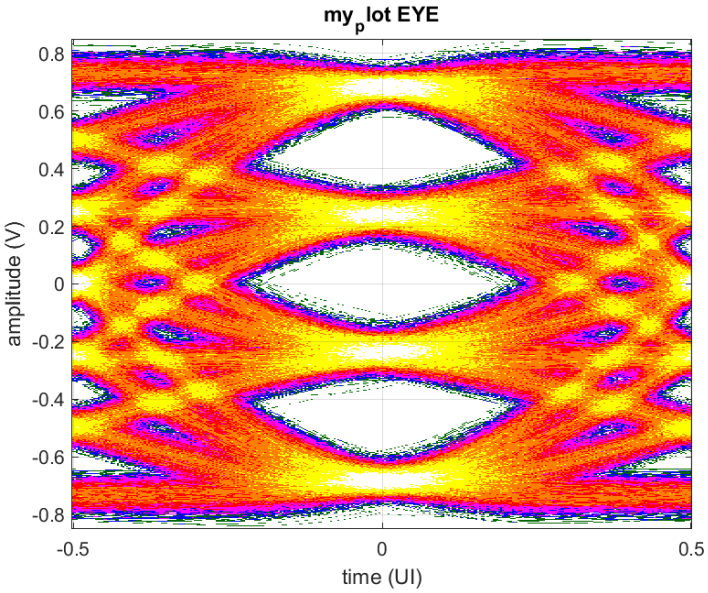

Figure 27 • Eye Diagram of PAM4

Note

The eye plot may take about 10 minutes to be generated, depending on the number of data samples. The eye diagram then appears in a popup window.

Chapter 8 : Speedster7t SerDes User Guide Revision History

Revision History

Version	Date	Description
1.0	09 Sep 2022	• Initial Release.
1.1	17 Aug 2023	• Minor changes to register addresses and content to match the updated XML database.
1.2	06 Nov 2023	• Remove references to end-of-life devices.
2.0	02 Jan 2025	• Added AC7t800 device information • Updated the latest ACE GUI capture • Added SerDes monitor (eye plot) information