

This document covers the PCIe configurations necessary for VectorPath Accelerator Cards.

PCIe IDs such as vendor ID, device ID, subsystem vendor ID, and subsystem ID must be set appropriately in the PCIe IP configuration for the device drivers to bind.

For correct PCIe enumeration, the Achronix Device Manager (ADM) must be included in a design. The data bus interface (DBI) gateway is part of the ADM. This gateway manages accesses from multiple sources (i.e., host software, ADM, fabric logic) which may need to access the PCIe DBI interface used for PCIe DMA, ATU, and MSI-X functions. The DBI gateway, besides accelerating the access to the DBI interface, also ensures atomic operation for each individual source, thus allowing multiple independent threads to simultaneously control and configure the PCIe core IP. DBI gateway configuration including associated BAR and ATU regions must be set in the PCIe IP configuration.

A remote procedure call (RPC) mechanism is supported in the ADM beginning with ACE version 10.4. The RPC mechanism allows both the PCIe host and FPGA fabric logic to invoke functions executed on the embedded MCU. This capability is particularly important for the AC7t700 AC7t1400 devices since direct access to the CSR address space is no longer supported [to ensure export restriction compliance](#), and these accesses must be performed through the ADM RPC function. An ATU region must be reserved for the RPC BRAM in the PCIe IP configuration.

PCIe design configuration options in ACE are specified in the ["PCI Express IP Configuration GUI interface"](#) chapter in the *Speedster7t PCIe User Guide User Guide* (UG098) (requires a support account to access).

PCIe Identifiers (IDs)

Description

PCIe device drivers are assigned to manage devices by the operating system using a process called [binding](#). Drivers bind to devices using rules based on the device's PCIe identifiers: the vendor ID, device ID, subsystem vendor ID, and subsystem ID. This mechanism allows multiple PCIe drivers to co-exist on the same system, each binding to its appropriate devices. Therefore, it is important that a device's PCIe identifiers match the binding rules used by the desired device driver.

The following tables list the ID values which are reserved for use with Achronix and BittWare cards and devices. These values should be used for designs that are intended to bind to either the Achronix or BittWare SDK device drivers, or in some designs, both device drivers.

Multiple Physical Functions

It is common to support multiple physical functions in a single PCIe design. Achronix reference and demo designs generally support two physical functions: pf0 for the Achronix or user design, and pf1 which contains the BittWare board management controller interface module (BW_BMC_IF). The BittWare physical function allows for BMC utilities, such as reading the temperature and build information, to be achieved over the PCIe bus.

These dual physical functions make it even more important to ensure that the correct values are used for each physical function. Typically the Achronix driver binds to pf0, and the BittWare driver binds to pf1.

PCIe IDs Explained

See https://en.wikipedia.org/wiki/PCI_configuration_space for a full explanation.

From the following identifiers, the device driver uses the vendor ID and device ID pair to determine whether to bind to each device probed during enumeration. The driver only binds to a device when both IDs match.

Further, it is possible, but optional, for the device driver to use the subsystem vendor and subsystem IDs to apply minor changes in operation between different products that have the same vendor ID and device ID.

Vendor ID (VID)

This value represents the manufacturer of the chipset. It applies regardless of the chipset type (ASIC or FPGA). In Achronix reference and demonstration designs, the Achronix physical function pf0 uses the Achronix vendor ID (`0x1b59`), and the BittWare physical function pf1 uses the BittWare vendor ID (`0x12ba`). See the vendor ID Values table below.

Device ID (DID)

This value is assigned by the vendor, and is used to identify a particular device or function from that vendor. In the case of an ASIC, the device ID normally identifies the ASIC. For an FPGA, the device ID can identify the FPGA or can be used to identify the board. Both Achronix and BittWare use device ID to identify the board. For example, Achronix uses `0x0010` for the S7t-VG6 VectorPath card. BittWare specifies various values from `0x0068` to `0x0075` to identify their cards, with `0x0069` applied to the S7t-VG6 VectorPath card. See the Device ID Values table below for additional examples.

Subsystem Vendor ID (SVID)

The SVID identifies the manufacturer of the design on the card. In Achronix reference and demo designs, the Achronix physical function has this value set to the Achronix vendor ID (`0x1b59`), and the BittWare physical function has this value set to the BittWare vendor ID (`0x12ba`).

Subsystem ID (SSID)

Subsystem ID, when used in conjunction with subsystem vendor ID, selects between different specific subsystems on the card. In the Achronix reference and demo designs this value identifies the specific design. BittWare use codes `0xb5d4` to `0xf5d6` for their designs, Achronix reserves `0xac10` to `0xacff` for their designs. See the Subsystem Vendor ID and Subsystem ID Values table below for a complete list.

Class Code

Although not used for binding or identifying the card and design, class codes indicate the overall product functionality. See the Class Code Values table below for the most common codes used by Achronix and BittWare designs.

Revision ID

This value specifies a revision identifier for a particular design. It is not currently used by any of the supported drivers, but is available for use by custom drivers and host-side software. It can be set to any value for the Achronix physical function, but must be set to `0x01` for the BittWare physical function.

PCIe ID Supported Values

Table 1 • Vendor ID Values

Vendor	Value
BittWare	<code>0x12ba</code>
Achronix	<code>0x1b59</code>

Table 2 • Device ID Values

Vendor	Board	Device ID
BittWare	S7t-VG6	<code>0x0069</code> ⁽¹⁾
BittWare	VP-815	<code>0x0079</code> ⁽¹⁾
BittWare	VP-708	<code>0x007a</code> ⁽¹⁾
Achronix	S7t-VG6	<code>0x0010</code> ⁽²⁾
Achronix	VP-815	<code>0x0012</code> ⁽²⁾
Achronix	VP-708	<code>0x0013</code> ⁽²⁾

Table Notes

1. BittWare reserves `0x0068` to `0x0075` for their various board products.
2. Achronix reserves `0x0010` to `0x0020` for their board products.

Table 3 • Subsystem Vendor ID and Subsystem ID Values

Subsystem Vendor ID	Subsystem ID ⁽¹⁾	Subsystem Design
BittWare	0xb5d4	Card test.
Achronix	0xac10	SDK design.
Achronix	0xac11	DMA bandwidth design.
Achronix	0xac12	Ethernet board link.
Achronix	0xac13	PCIe, DDR4 and Ethernet.
Achronix	0xac14	Multi-IP.
Achronix	0xac15	Bitfile licensing.
Achronix	0xac16	Partial Reconfiguration.

Table Notes

1. BittWare reserves a range of subsystem IDs, from 0xb5d4 to 0xf5d6 . 0xb5d4 is recommended for use with the BW_BMC_IF logic which is added to any VectorPath design.

Table 4 • Class Code Values

Code	Type
0x12	Processing accelerators. All Achronix physical functions are set to this value.
0x13	Non essential instrumentation. All BittWare designs and physical functions use this value.

Achronix Reference/Demo Design PCIe IDs

The following tables summarizes the PCIe IDs used for the Achronix and BittWare physical functions in the most common Achronix reference and demonstration designs.

Table 5 • PCIe Identifiers for Achronix Physical Functions

Design Name	Physical Function	Vendor ID (VID)	Device ID (DID) ^(1,2)	Subsystem Vendor ID (SVID)	Subsystem ID (SSID)	Class Code
Achronix SDK design	pf0	0x1b59	0x0010	0x1b59	0xac10	0x12
PCIe DMA bandwidth design	pf0	0x1b59	0x0010	0x1b59	0xac11	0x12
Ethernet board link design	pf0	0x1b59	0x0010	0x1b59	0xac12	0x12
PCIe, DDR4 and Ethernet combined demo design	pf0	0x1b59	0x0010	0x1b59	0xac13	0x12
Multi-IP reference design	pf0	0x1b59	0x0010	0x1b59	0xac14	0x12
Bitfile licensing design	pf0	0x1b59	0x0010	0x1b59	0xac15	0x12
Partial Reconfiguration design	pf0	0x1b59	0x0010	0x1b59	0xac16	0x12

Table Notes

1. If the design is targeted to a VectorPath VP815 card with a Speedster7t AC7t1500 device, per the Device IDs table, the value of 0x0012 should be used.
2. If the design is targeted to a VectorPath VP708 card with a Speedster7t AC7t800 device, per the Device IDs table, the value of 0x0013 should be used.

Table 6 • PCIe Identifiers for BittWare Physical Functions

Design Name	Physical Function	Vendor ID (VID)	Device ID (DID)	Subsystem Vendor ID (SVID)	Subsystem ID (SSID)	Class Code
BW_BMC_IF Macro	pf1	0x12ba	0x0069	0x12ba	0xb5d4	0x13

Device Driver Binding Rules

Each device driver makes binding decisions based on its own binding rules and conventions. Be sure to understand the binding rules of the selected driver(s).

Achronix PCIe Driver

The Achronix driver binds to devices based on their vendor and device IDs. The other IDs are ignored.

By default, the Achronix driver binds to devices with vendor ID 0x1b59 (Achronix), and device IDs in the *Device ID Values* table. But those values are easily changed by modifying the driver source code.

BittWare BWPCI Driver

In versions of the BittWare SDK older than 2024.3.1, the BittWare driver uses binding rules based on all four of the IDs: the vendor ID, device ID, subsystem vendor ID, and subsystem ID.

The BWPCI driver is hard coded to bind to devices with vendor ID 0x12ba (BittWare), device IDs between 0x0068 and 0x0075, and subsystem vendor IDs 0x12ba (BittWare) and 0x1b59 (Achronix), and subsystem IDs between 0xb5d4 to 0xf5d6. 0xb5d4.

BittWare BWVFIO Driver

In versions of the BittWare SDK 2024.3.1 and newer, the BittWare SDK uses the built-in Linux VFIO driver. It binds based on UDEV rules in the file `/etc/udev/rules.d/99-bwvfio.rules`, which are populated by the SDK's installer. Those UDEV rules use the vendor ID, subsystem vendor ID, and subsystem ID. The device ID is ignored.

The BWVFIO driver's UDEV rules bind to devices with vendor ID 0x12ba (BittWare), subsystem vendor IDs 0x12ba (BittWare) and 0x1b59 (Achronix), and subsystem IDs 0xb5d4 to 0xf5d6.

Example

Using the Achronix SDK demo design, *acx_sdk_vp_demo*, as an example, the following is required when configuring the PCIe IP core in ACE versions 10.0 and later.

Overview

The overall configuration of the PCIe IP is shown in the following figures.

The screenshot displays the 'Speedster7t PCI Express' configuration window. The title bar shows 'pci_express_x16.acxip'. The main header is green with the text 'Speedster7t PCI Express' and 'Overview'. Below the header, a description states: 'This page contains the top-level, global properties that govern the structure and base configuration of the PCI Express Interface wrapper.'

The configuration is organized into several sections, each with a green checkmark icon:

- Target Device:** AC7t1500
- PCIe Placement:** PCIE_1
- PCIe Version:** Gen 5
- Operating Mode:** Endpoint
- Number of Lanes:** 16

PCIe Clock Settings:

- AXI Master Clock Name:** i_pcie_ts_clk
- AXI Master Clock Frequency:** 1000.0 MHz
- AXI Slave Clock Name:** i_pcie_ts_clk
- AXI Slave Clock Frequency:** 1000.0 MHz
- AUX Clock Name:** i_pcie_ts_clk
- AUX Clock Frequency:** 1000.0 MHz

PMA Clock Settings:

- Enable PMA Ref Clock Sharing:** ☒
- Master Ref Clock Ball Name:** SRDS_N1_REFCLK_P

Manual Lane Flip:

- Force Lane Flip:** ☐
- Physical Lane Number:** 0

Number of Physical Functions: 2

At the bottom, there is a help icon (question mark), a 'Generate' button, and 'Back' and 'Next' navigation buttons.

Figure 1 • PCIe Configuration Overview

Achronix Physical Function (PF0)

pci_express_x16.acxip x

Speedster7t PCI Express

Physical Function 0
This page contains the top-level settings for this Physical Function

✓ PF0 Device ID (hex)	0010
✓ PF0 Revision ID (hex)	37
✓ Vendor ID (hex)	1b59
✓ PF0 Subsystem ID (hex)	ac10
✓ Subsystem Vendor ID (hex)	1b59
✓ PF0 Class Code (hex)	12
✓ ☒ Enable MSI-X Capability	

Configuration | File Preview

Generate << Back Next >>

Figure 2 • PCIe Configuration PF0

Settings

- **PF0 Device ID** – 0x0010 , the Achronix VectorPath S7t-VG6 board
- **PF0 Revision ID*** – 0x37 , the current revision identifier for the design
- **PF0 Vendor ID** – 0x1b59 , the Achronix vendor ID
- **PF0 Subsystem ID*** – 0xac10 , the Achronix SDK demo design
- **PF0 Subsystem Vendor ID*** – 0x1b59 , the Achronix vendor ID
- **PF0 Class Code*** – 0x12 , defined as a processing accelerator

Note

Fields marked with an asterisk (*) are not used by the Achronix PCIe driver, but are available for use by custom drivers.

BittWare Physical Function

Speedster7t PCI Express

Physical Function 1
This page contains the top-level settings for this Physical Function

- ✓ PF1 Device ID (hex)
- ✓ PF1 Revision ID (hex)
- ✓ Vendor ID (hex)
- ✓ PF1 Subsystem ID (hex)
- ✓ Subsystem Vendor ID (hex)
- ✓ PF1 Class Code (hex)
- ✓ ☐ Enable MSI-X Capability

? Generate << Back Next >>

Configuration File Preview

Figure 3 • PCIe Configuration PF1

Settings

- **PF1 Device ID** – `0x0069`, the BittWare VectorPath board.
- **PF1 Revision ID** – `0x01`, as required by the BittWare PCIe device driver.
- **PF1 Vendor ID** – `0x12ba`, the BittWare vendor ID.
- **PF1 Subsystem ID** – `0xb5d4`, the BittWare card test design.
- **PF1 Subsystem Vendor ID** – `0x12ba`, the BittWare vendor ID.
- **PF1 Class Code** – `0x13`, defined as Non-Essential Instrumentation.

NAP Addresses

Associated with PCIe configuration, it is necessary when defining the PCIe IP to define the base address register (BAR) target address mappings. Often a BAR is mapped to a set of hard IP configuration and status registers, or a NAP in the fabric or. Frequently that NAP provides the control plane to the design using the `reg_control_block` module.

As an example, NAP locations and their associated BAR addresses for the demo design `acx_sdk_vp_demo` are listed in the following table.

Table 7 • Example NAP Addresses

NAP Column	NAP Row	2D NoC Address	Comment
5	5	<code>0x42_4000_0000</code>	<code>reg_control_block</code> location.
5	7	<code>0x42_6000_0000</code>	MSI-X Interrupt Handler
9	2	<code>0x44_1000_0000</code>	Default address for the BittWare BMC module.
9	8	<code>0x44_7000_0000</code>	Function Level Reset
7	7	<code>0x43_6000_0000</code>	BRAM
8	7	<code>0x43_e000_0000</code>	BRAM DMA
9	7	<code>0x44_6000_0000</code>	BRAM descriptor lists
6	4	<code>0x42_b000_0000</code>	ADM location.

Calculating NAP Addresses

To convert from a NAP location to a 2D NoC address on the Speedster7t AC7t1500 FPGA, use the following equation:

$$\text{Address} = 0x40_0000_0000 + ((\text{COLUMN} - 1) \ll 31) + ((\text{ROW} - 1) \ll 28)$$

When configuring the DBI gateway or RPC BRAM ATU settings (see next section), it is necessary to know the NAP address of the ADM.

ADM Configuration

As explained in the introduction, it is necessary to include the Achronix Speedster7t Device Manager (ADM) in any PCIe design using a VectorPath card with a Speedster7t AC7t1500 or AC7t1400 FPGA. The ADM should be configured as shown in the following figure.

Note

In ACE releases previous to ACE 10.2, to enable the DBI gateway in the Device Manager, select the Enable PCIE_0 DBI Gateway option or Enable PCIE_1 DBI Gateway option in the ACE Speedster7t Device Manager Configuration Editor. Enable PCIE_0 DBI Gateway option must be selected for PCIE_0 (PCIe ×8) DBI access, while Enable PCIE_1 DBI Gateway option must be selected for PCIE_1 (PCIe ×16) DBI access.

The screenshot shows the 'Speedster7t Device Manager' configuration window. The 'Overview' section states: 'This page contains the top-level, global properties that govern the structure and base configuration of the Device Manager wrapper.' Below this, several configuration options are listed with green checkmarks indicating they are enabled or valid:

- Target Device: AC7t1500
- NAP Row: 4
- NAP Column: 6
- ☐ Enable PCIE_0 Support
- ☒ Enable PCIE_1 Support
- ☐ Enable ETH_0 Quad 0 ANLT
- ☐ Enable ETH_0 Quad 1 ANLT
- ☐ Enable ETH_1 Quad 0 ANLT
- ☐ Enable ETH_1 Quad 1 ANLT

At the bottom, there are buttons for '?', 'Generate', '<< Back', and 'Next >>'. The 'Configuration' tab is selected in the bottom navigation bar.

Figure 4 • ADM Configuration

The ADM NAP location is set in the ADM IP configuration GUI interface in ACE. In this example, the ADM is set to column 6, row 4. The corresponding NAP address is `0x42_b000_0000`. This address is used elsewhere in the configuration of the PCIe BAR, which is set for access to the DBI gateway and the RPC BRAM region.

DBI Gateway ATU Regions

To allow access for host software to communicate with the DBI gateway, it is necessary to configure one PCIe BAR assigning it to the NAP address space of the ADM. Further, this BAR should then be configured in address match mode, with two ATU regions mapped to the DBI Gateway. Achronix has selected BAR 3 as the usual BAR for access

to the DBI gateway, although any available BAR could be used. For more information about the DBI Gateway see the knowledge base article, [What is the DBI Gateway and How Can I Use It?](#)

Using this ADM configuration, with a NAP address of `0x42_b000_0000`, the following configuration should be set for BAR 3.

The screenshot shows the 'Speedster7t PCI Express' configuration window. The 'PF0 Memory Map' section is active, displaying the 'BAR3' configuration. The settings are as follows:

PF0 BAR3 Function	NoC
✓ ☒ BAR3 Enabled	
✓ BAR3 User-Defined Label	PF0_BAR3_AMM
✓ BAR3 Width	32-bit
✓ BAR3 Type	Memory
✓ BAR3 Size (Bytes)	1M
✓ ☐ BAR3 Prefetchable	
✓ BAR3 Address Mode	Address Match Mode
✓ BAR3 NoC Address Value (hex)	02000000000
✓ BAR3 Number of ATU Regions	4

At the bottom of the window, there are buttons for 'Generate', '<< Back', and 'Next >>'. The 'Configuration' tab is selected at the bottom left.

Figure 5 • BAR 3 Configuration

The DBI gateway requires two ATU regions:

- 64KB address to the ADM NAP location
- 128K addressed to the ADM NAP location + `0x30_0000`

The configuration of these two regions is show in the following figure.

pci_express_x16.acxip x

Speedster7t PCI Express

PF0 BAR3 ATU Regions
This page contains the properties for the PCIe ATU regions in Address Match Mode

PF0 BAR3 Region 0

- ✓ User-Defined Label: PF0_BAR3_0_NAP64_DBIGW_PCIE
- ✓ Absolute Region Number: 3
- BAR Offset (hex): 0000000000000000
- ✓ Size Multiple: 1
- Region Size (Bytes): 65536
- ✓ NoC Start Address (hex): 042b000000
- ✓ NoC End Address (hex): 042b000ffff

PF0 BAR3 Region 1

- ✓ User-Defined Label: PF0_BAR3_1_NAP64_DBIGW_ATUDMA
- ✓ Absolute Region Number: 4
- BAR Offset (hex): 0000000000010000
- ✓ Size Multiple: 2
- Region Size (Bytes): 131072
- ✓ NoC Start Address (hex): 042b030000
- ✓ NoC End Address (hex): 042b031ffff

Configuration File Preview

Generate << Back Next >>

Figure 6 • BAR 3 ATU Region Configuration for DBI

RPC BRAM ATU Region

RPCs can be invoked from host software or FPGA logic to perform tasks such as switching SerDes operating rate or trigger link training. To allow access for host software to communicate with the RPC block, as with the DBI Gateway, it is necessary to configure a PCIe BAR assigning it to the NAP address space of the ADM. One ATU region is required, which can be in the same BAR as the DBI gateway.

The RPC BRAM region requires one ATU region –64K addressed to the ADM NAP location + `0x88_0000`

Using this ADM configuration, with a NAP address of `0x42_b000_0000`, the following configuration should be set for BAR 3.

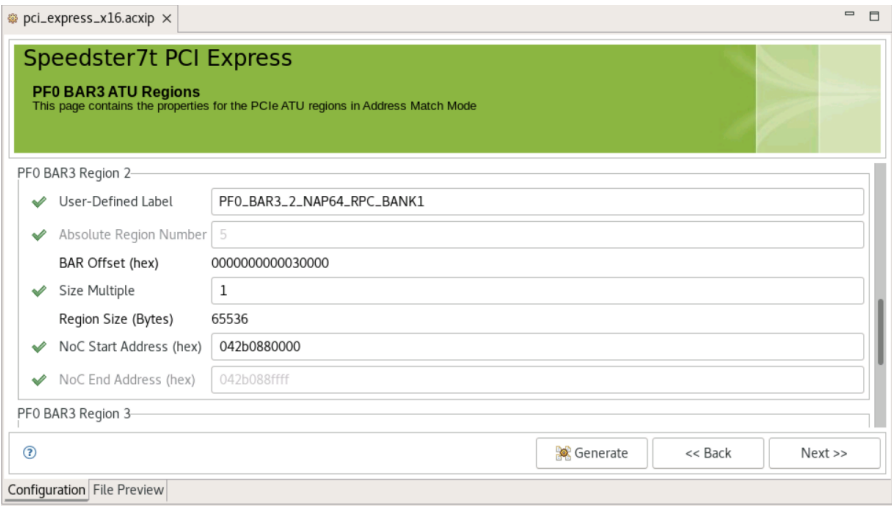


Figure 7 • BAR 3 ATU Region Configuration for RPC

Summary

For successful enumeration and binding to the a device driver, it is necessary to correctly configure the PCIe IP core to the appropriate device and vendor IDs.

To run DMA, configure ATU regions, perform RPC functions, and handle MSI-X interrupts, the ADM with DBI gateway and RPC BRAM must be included. The host software access must be configured using a combination of BARs and ATU regions.

Revision History

Version	Date	Description
1.0	 03 Nov 2025	• Initial Achronix Release. Replaces the KBA on the same topic.



Achronix Semiconductor Corporation

2903 Bunker Hill Lane
Santa Clara, CA 95054
USA

Website: www.achronix.com
E-mail : info@achronix.com

Copyright © 2025 Achronix Semiconductor Corporation. All rights reserved. Achronix, Speedster and VectorPath are registered trademarks, and Speedcore and Speedchip are trademarks of Achronix Semiconductor Corporation. All other trademarks are the property of their prospective owners. All specifications subject to change without notice.

Notice of Disclaimer

The information given in this document is believed to be accurate and reliable. However, Achronix Semiconductor Corporation does not give any representations or warranties as to the completeness or accuracy of such information and shall have no liability for the use of the information contained herein. Achronix Semiconductor Corporation reserves the right to make changes to this document and the information contained herein at any time and without notice. All Achronix trademarks, registered trademarks, disclaimers and patents are listed at www.achronix.com/legal.